SYSTEM BLOCK DIAGRAM

A560_27IOB

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P77 PCH GPIO Table
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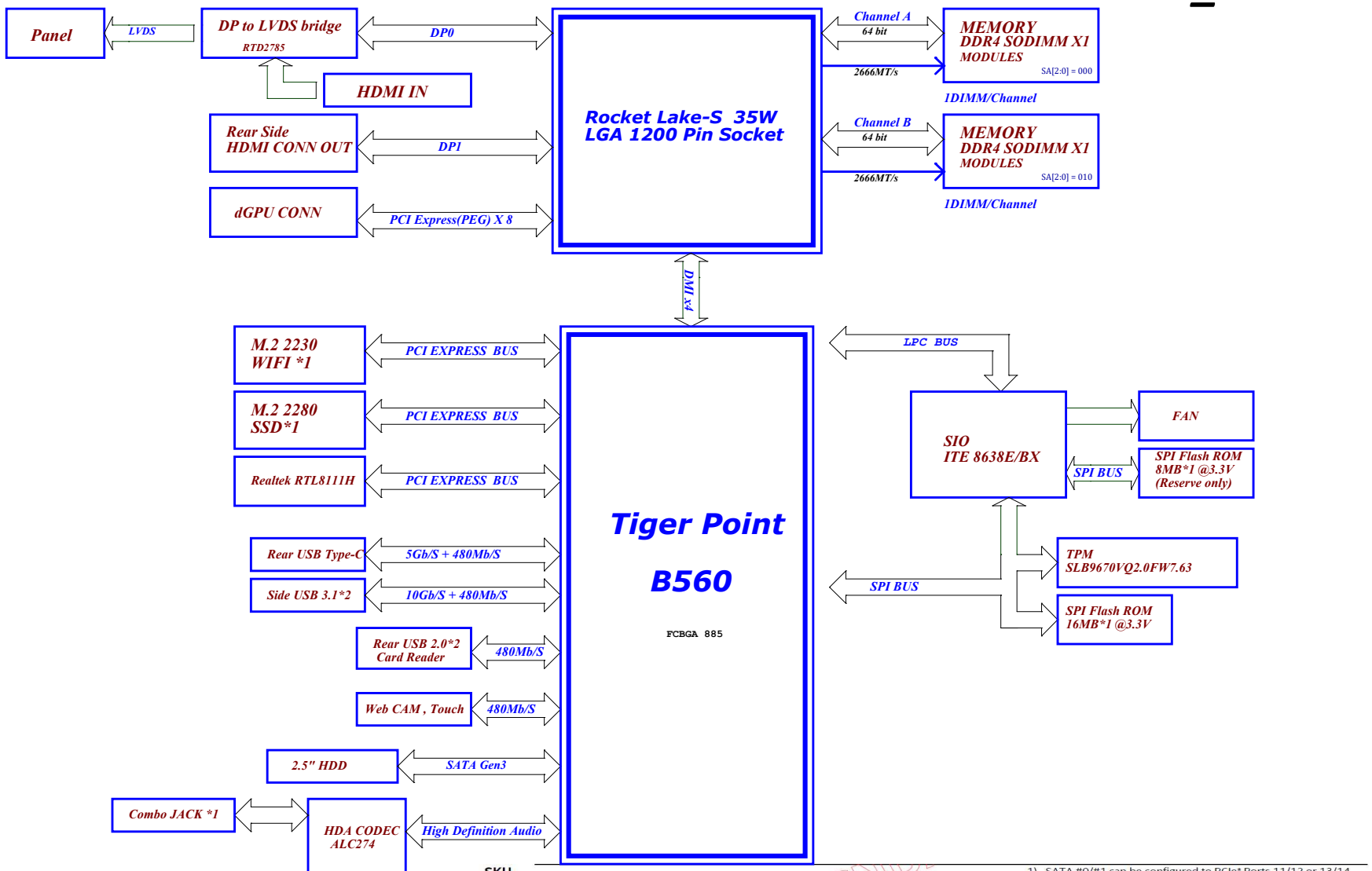

SKU

1) SATA #0/#1 can be configured to PCIe* Ports 11/12 or 13/14.

SKU																															
H510	USB3.2 Gen 1x1	USB3.2 Gen 1x1	USB3.2 Gen 1x1	USB3.2 Gen 1x1	N/A	N/A	N/A	N/A	N/A	N/A	PCIe LAN	PCIe	PCIe	PCIe	PCIe	LAN Only	N/A	PCIe	PCIe LAN	SATA LAN	SATA	SATA	SATA	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
B560	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen 1x1	USB3.2 Gen 1x1	N/A	N/A	N/A	N/A	PCIe LAN	PCIe	PCIe	PCIe	PCIe	PCIe LAN	PCIe	PCIe SATA	PCIe SATA LAN	SATA LAN	SATA	SATA	SATA	SATA	SATA	N/A	N/A	PCIe	PCIe	PCIe	PCIe
H570	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen 1x1	USB3.2 Gen 1x1	USB3.2 Gen 1x1	USB3.2 Gen 1x1	PCIe	PCIe	PCIe LAN	PCIe	PCIe	PCIe	PCIe	PCIe LAN	PCIe	PCIe SATA	PCIe SATA LAN	PCIe SATA LAN	PCIe SATA	PCIe SATA	PCIe SATA	SATA	SATA	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe
Q570	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen1x1	USB3.2 Gen1x1	PCIe LAN	PCIe	PCIe	PCIe	PCIe	PCIe LAN	PCIe	PCIe SATA	PCIe SATA LAN	PCIe SATA LAN	PCIe SATA	PCIe SATA	PCIe SATA	PCIe SATA	PCIe SATA	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe
Z590	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	PCIe LAN	PCIe	PCIe	PCIe	PCIe	PCIe LAN	PCIe	PCIe SATA	PCIe SATA LAN	PCIe SATA LAN	PCIe SATA	PCIe SATA	PCIe SATA	PCIe SATA	PCIe SATA	PCIe	PCIe	PCIe	PCIe	PCIe	PCIe
W580	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	USB3.2 Gen2x1	PCIe LAN	PCIe	PCIe	PCIe	PCIe	PCIe LAN	PCIe	PCIe SATA	PCIe SATA LAN	PCIe SATA LAN	PCIe SATA	PCIe SATA	PCIe SATA	PCIe SATA	PCIe SATA	PCIe SATA	PCIe SATA	PCIe SATA	PCIe	PCIe	PCIe	PCIe

Intel confidential

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Title	P01 Block Diagram
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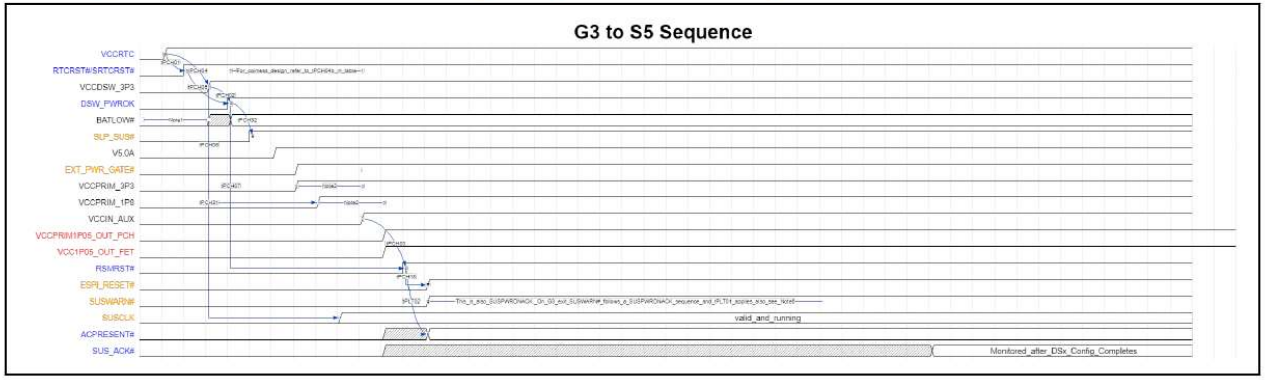
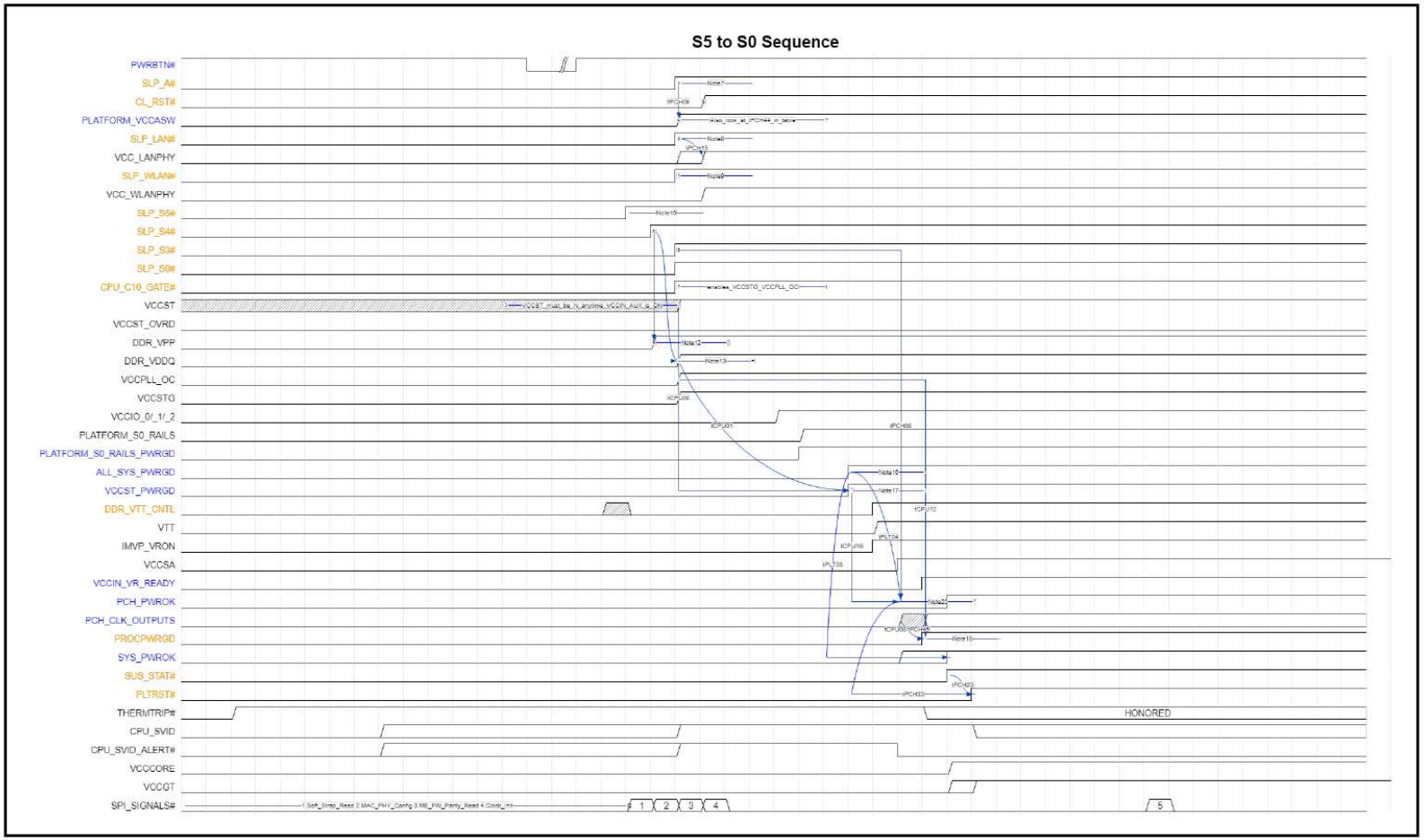
Timing Diagram for G3 to S0 [Deep Sx Platform]

G3 to S5 Sequence



S5 to S0 Sequence



Asia Vital Components Co., Ltd.		
Title: P02 POWER Sequence(G3-S0)		
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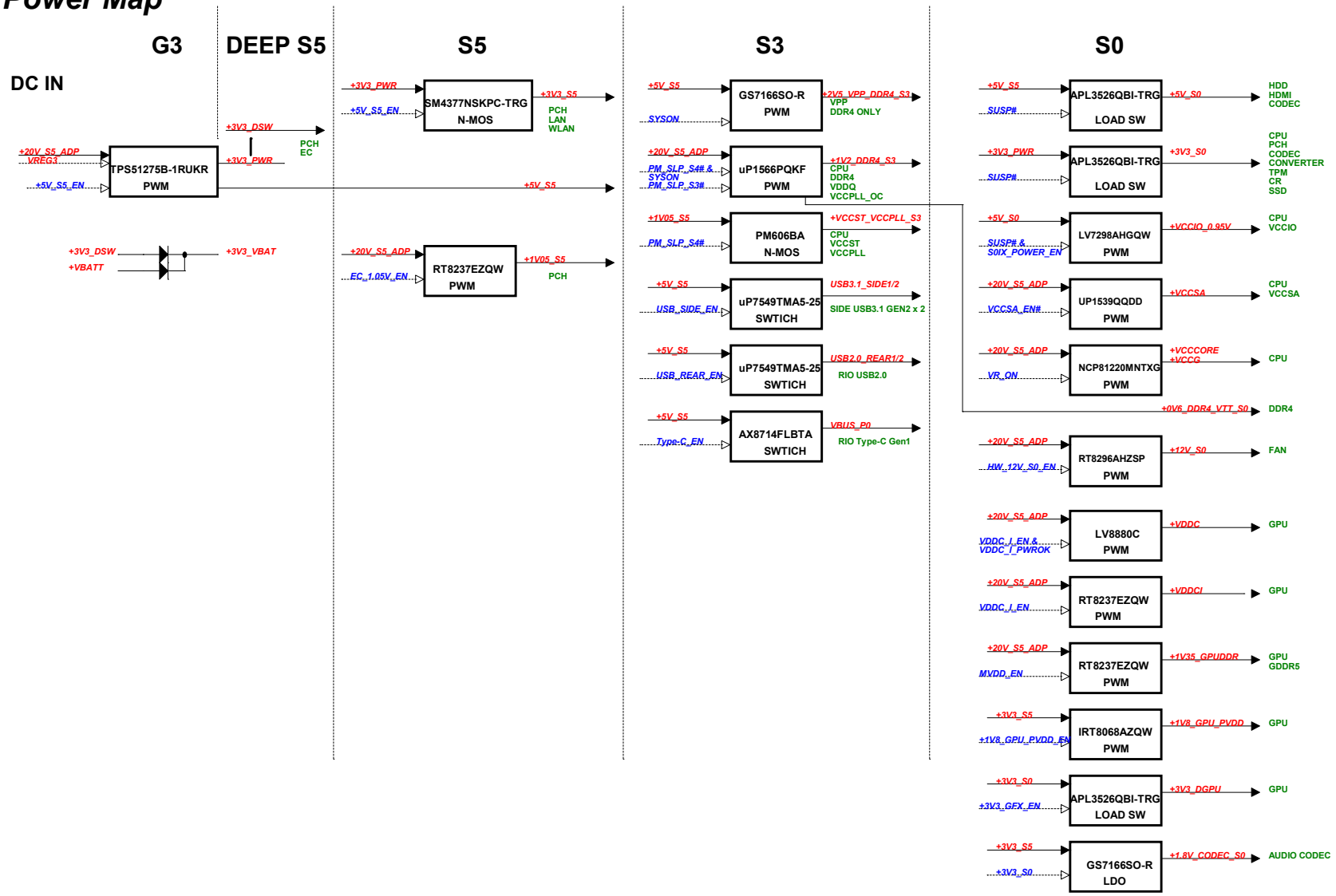
Power Map



Asia Vital Components Co., Ltd.			
Title: P03 Power Map			
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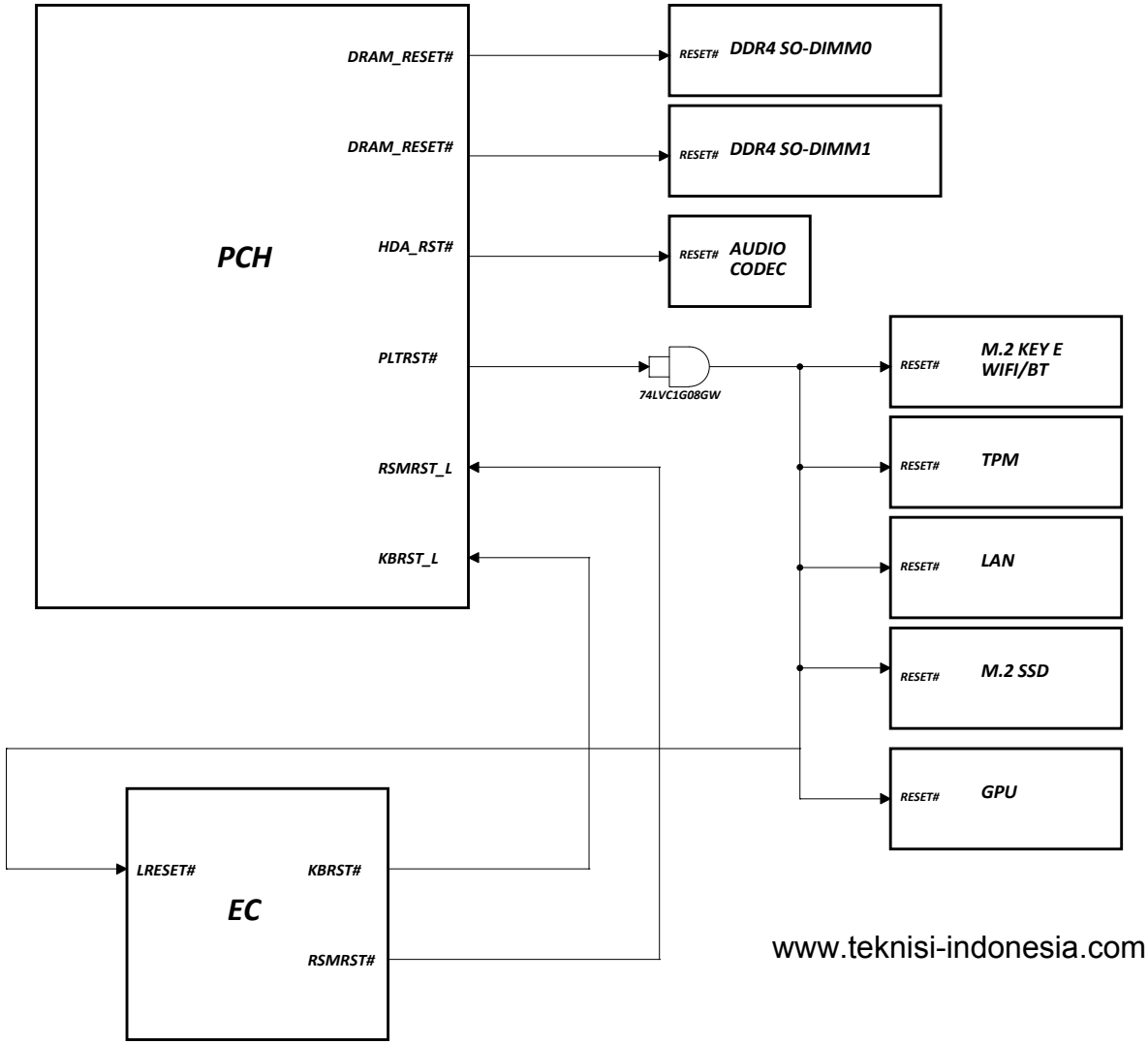
RST MAP



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Title: P04 RESET MAP		
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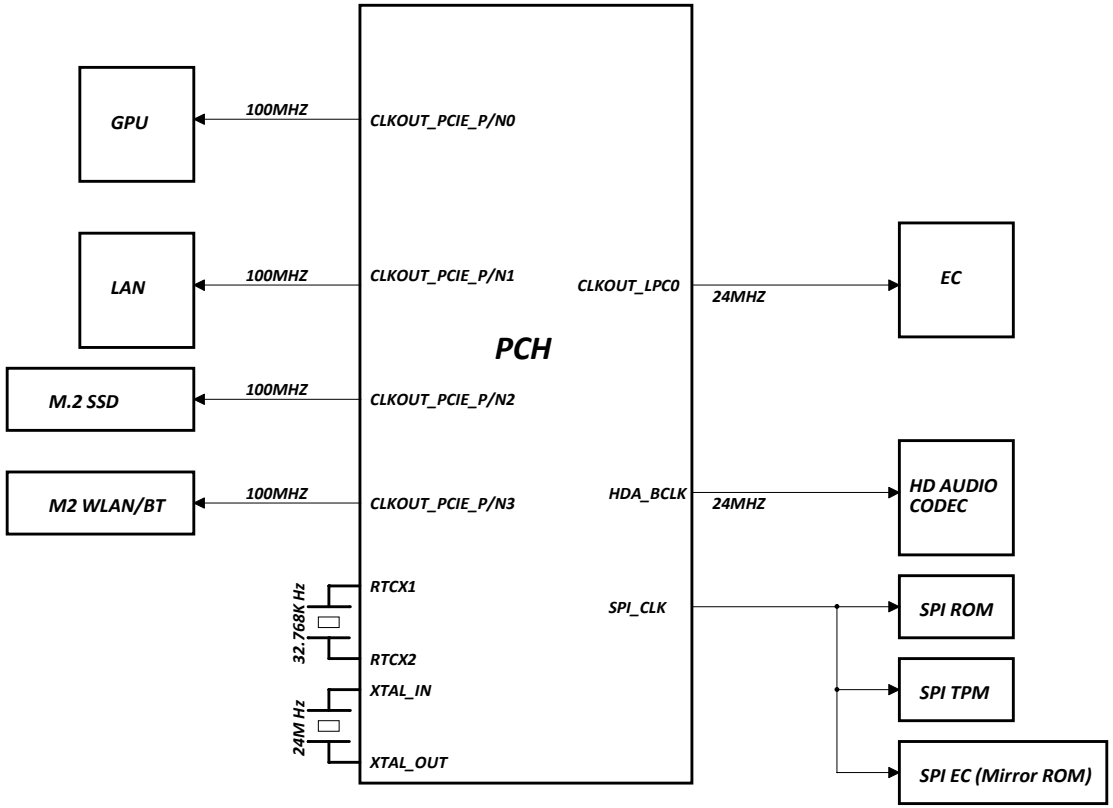
CLOCKS DIAGRAM



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Title: P05 CLOCK DIAGRAM		
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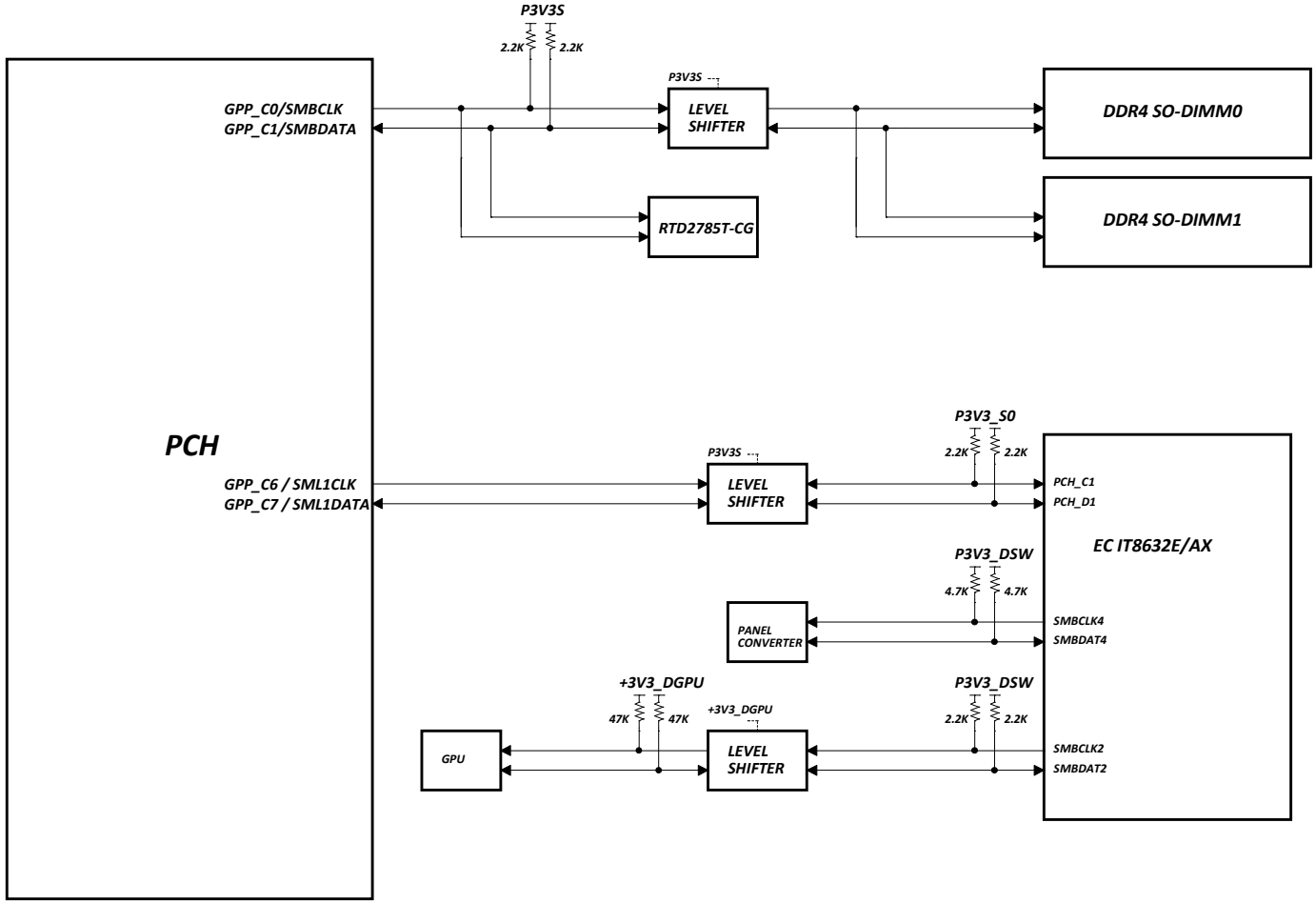
SMBus MAP



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Title: P06 SMBUS MAP		
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HW STRAPING

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Title: P07 HW STRAPING		
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RESERVED

Asia Vital Components Co., Ltd.		
Title: P08 RESERVED		
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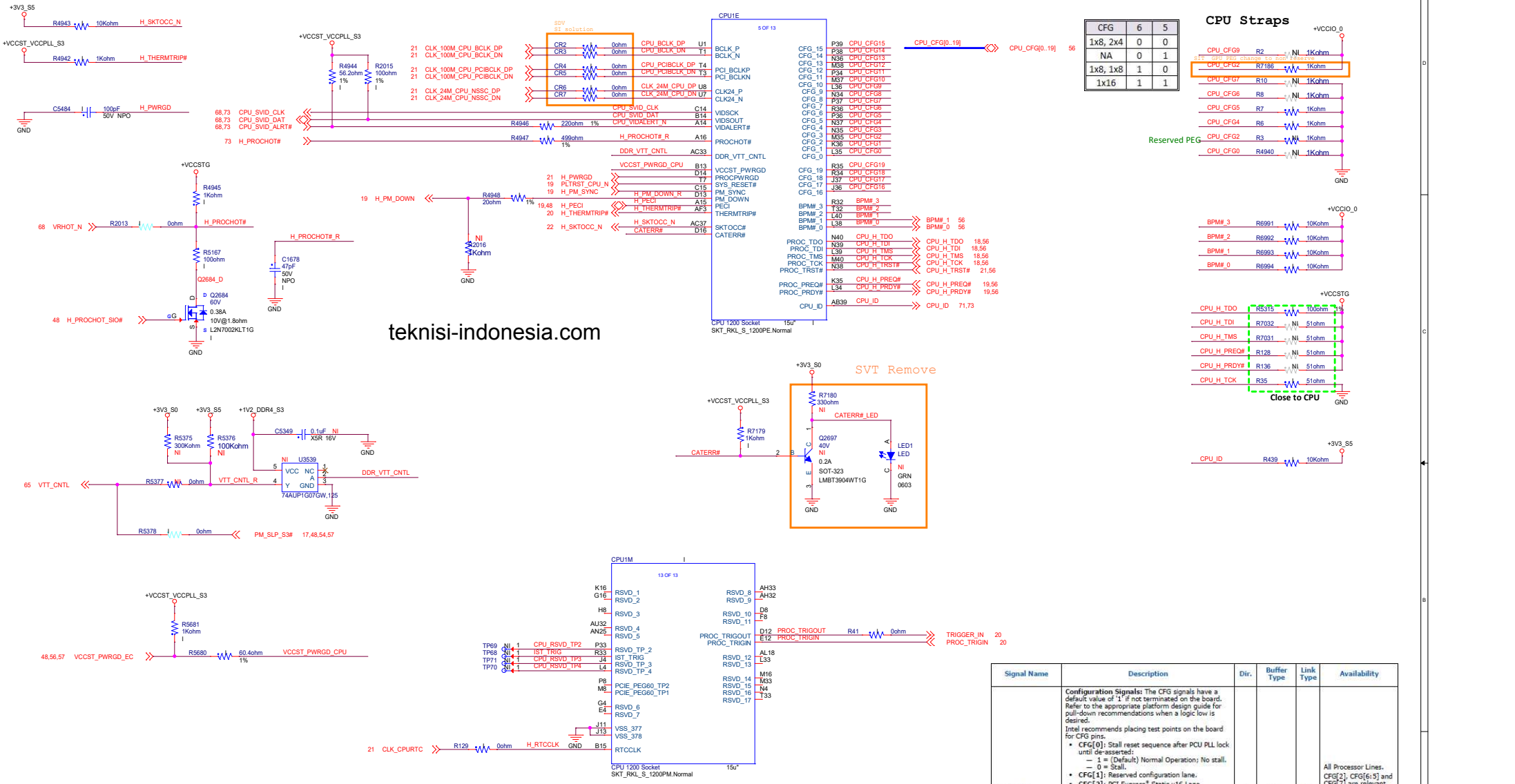

CFG	6	5
1x8, 2x4	0	0
NA	0	1
1x8, 1x8	1	0
1x16	1	1

Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
CFG[15:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. Intel recommends placing test points on the board for CFG pins. • **CFG[0]:** Stall reset sequence after PCU PLL lock until de-asserted: — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • **CFG[1]:** Reserved configuration lane. • **CFG[2]:** PCI Express* Static x16 Lane Numbering Reversal. — 1 = Normal operation — 0 = Lane numbers reversed. • **CFG[3]:** Reserved configuration lane. • **CFG[4]:** eDP enable: — 1 = Disabled. — 0 = Enabled. • **CFG[6:5]:** PCI Express* Bifurcation — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • **CFG[15:7]:** Reserved configuration lanes.	I	GTL	SE	All Processor Lines. CFG[2], CFG[6:5] and CFG[7] are relevant for S Processor Line only and test point may be placed on the board for them.
CFG[16P,17P] CFG[16N,17N]	• Reserved configuration lanes. • Reserved configuration lanes.	I	GTL	SW	

Asia Vital Components Co., Ltd.

Title: P09 CPU (CLK,CFG,VID,DEBUG)

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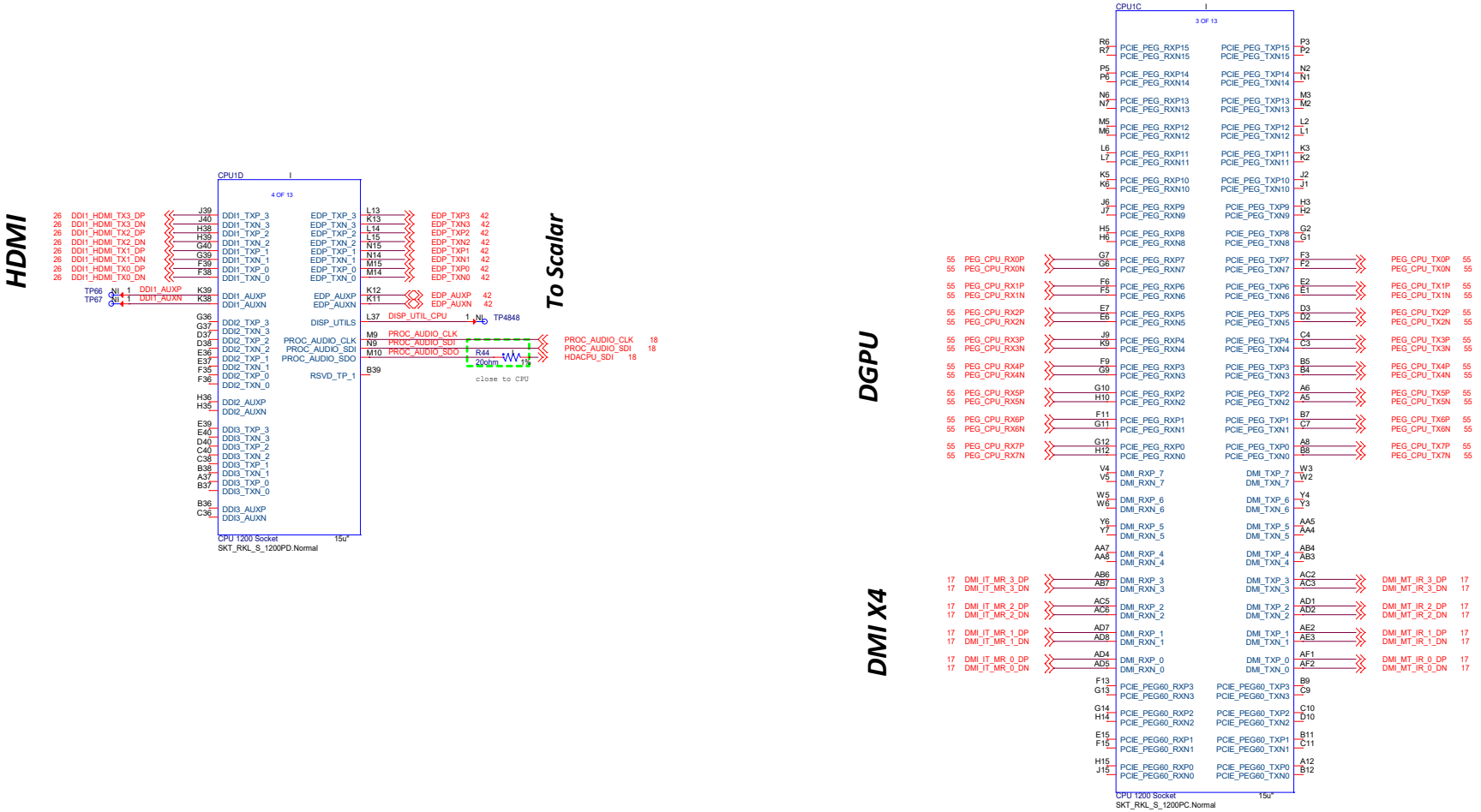
CPU - EDP / DDI / PEG



Asia Vital Components Co., Ltd.	
Title: P10 CPU - EDP, DDI, PEG,	
Size: C	Document Number: A560-27IOB
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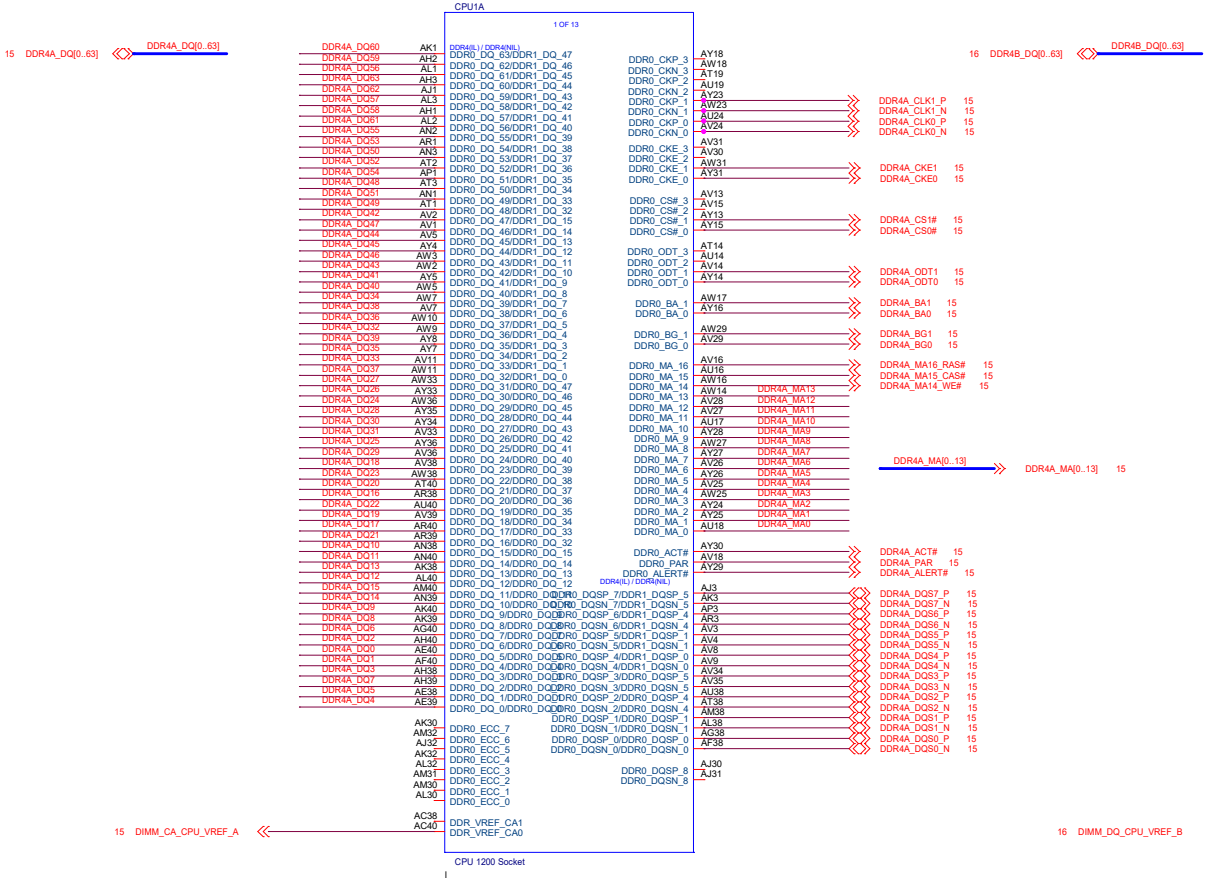
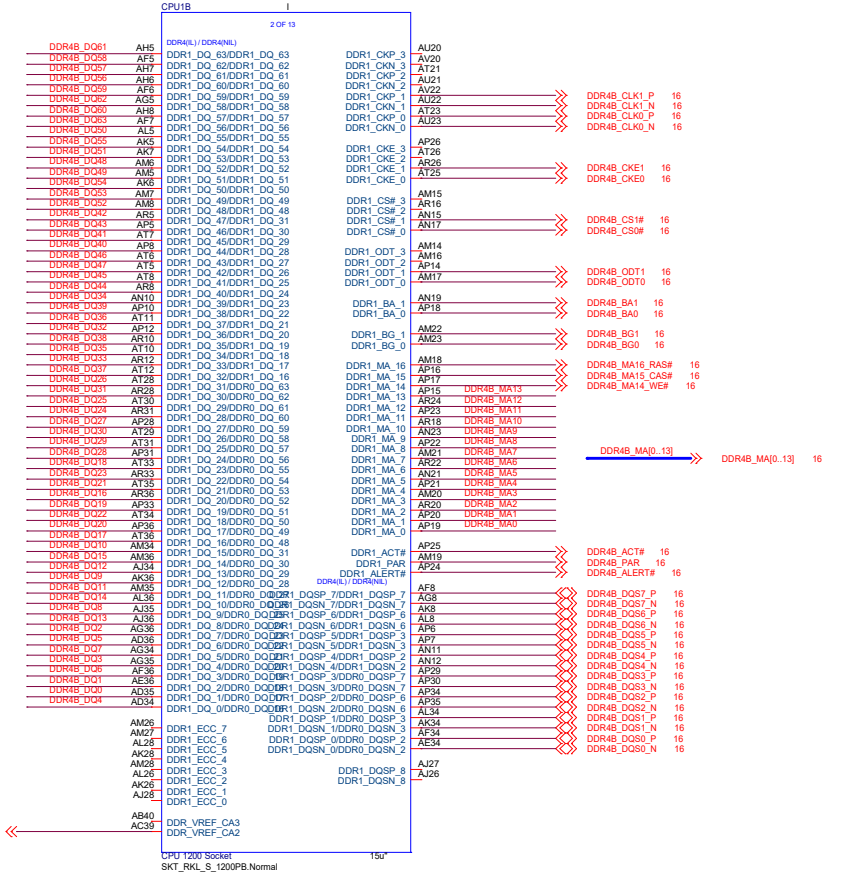
CPU DDR4 CHA



CPU DDR4 CHB



Asia Vital Components Co., Ltd.			
Title: P11 CPU - DDR4			
Size: C	Document Number: A560-27IOB		Rev: X03
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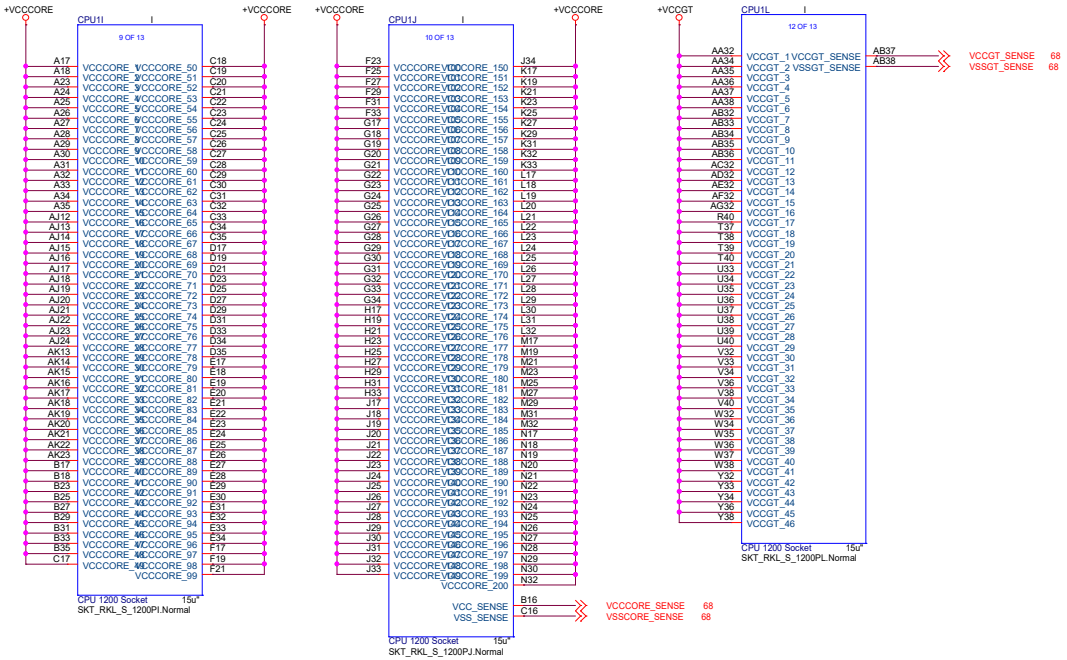

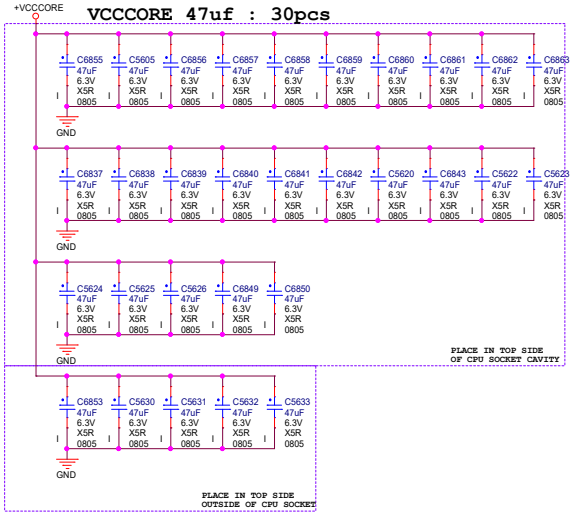

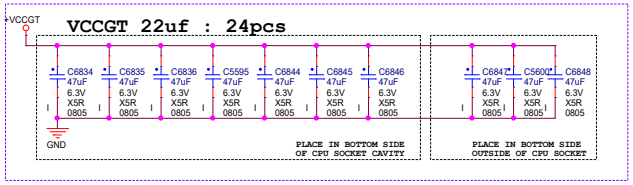

Asia Vital Components Co., Ltd.			
Title: P12 CPU - VCORE, GT			
Size: C	Document Number: A560-2710B		Rev: X03
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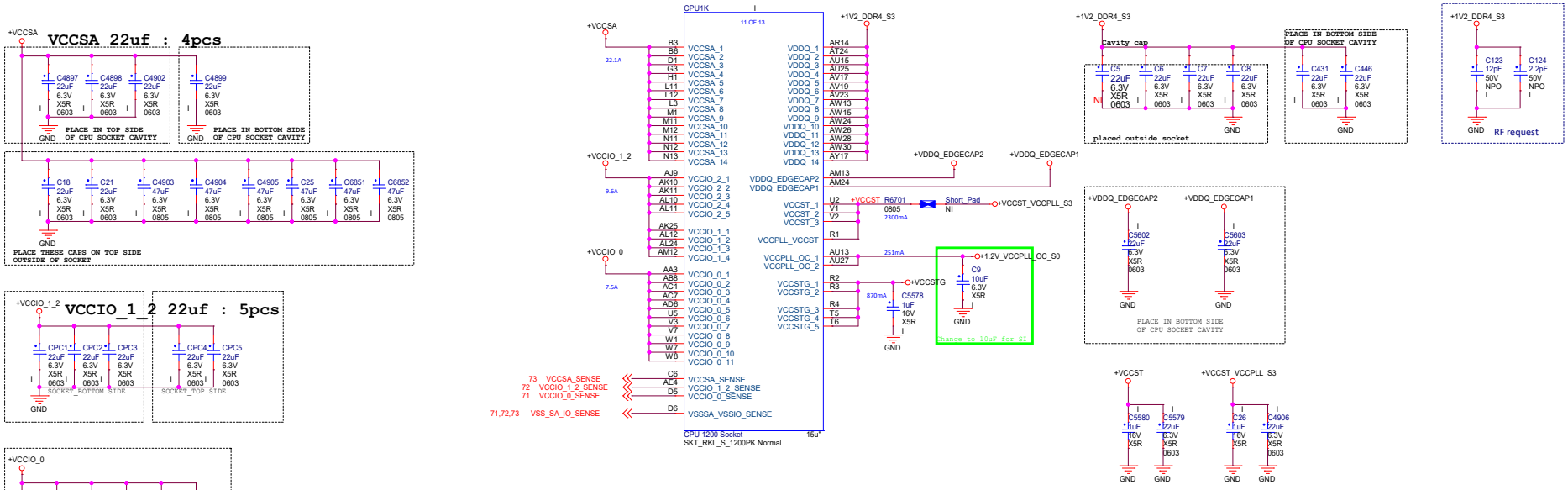
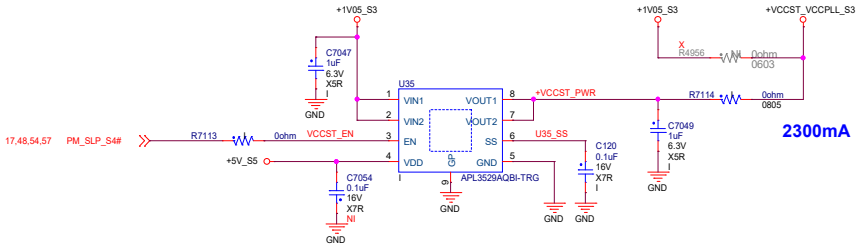
CPU - VDDQ / SA / IO / VCCSTG



+VCCST_VCCPLL_S3



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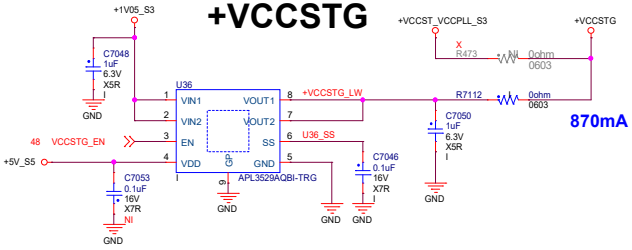
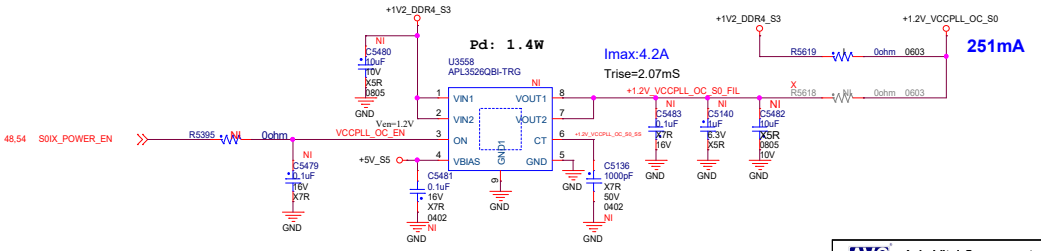
+VCCSTG



+1.2V_VCCPLL_OC



Asia Vital Components Co., Ltd.	
Title: P13 CPU - VDDQ, SA, IO, VCCSTG	
Size: C	Document Number: A560-27IOB
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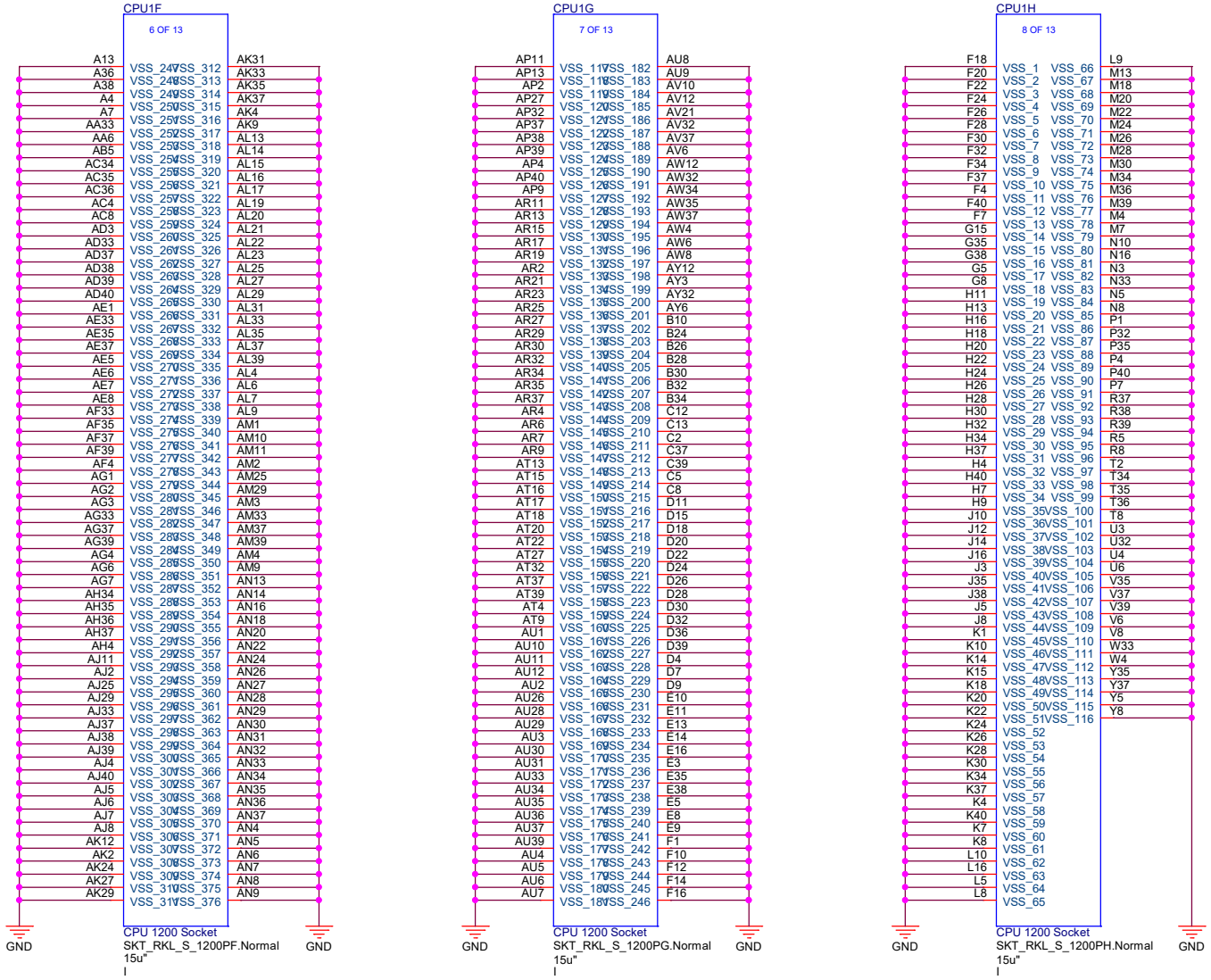

AVC Asia Vital Components Co., Ltd.		
Title: P14 CPU - VSS		
Size: B	Document Number: A560-27IOB	Rev: X03
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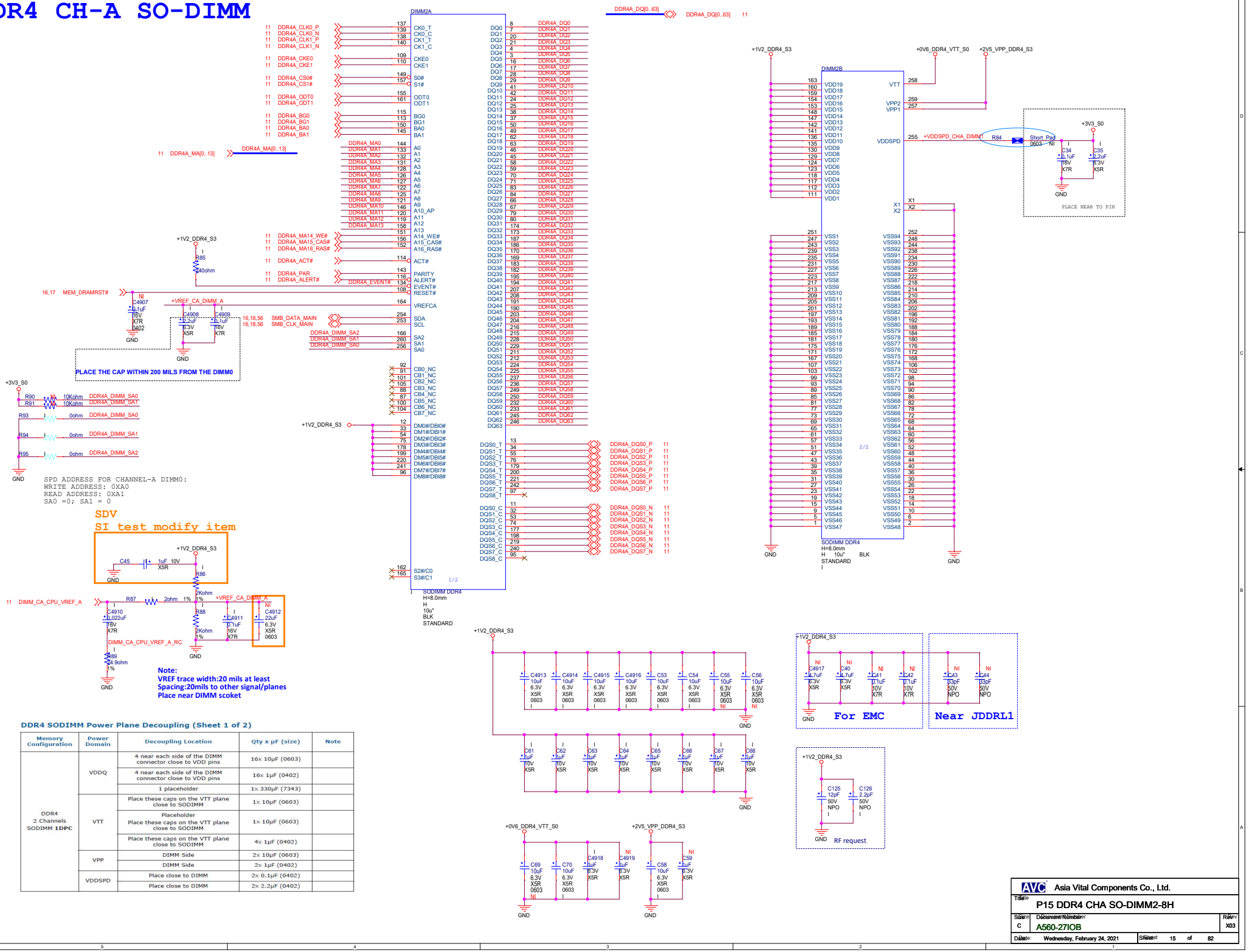
DDR4 CH-A SO-DIMM



DDR4 SODIMM Power Plane Decoupling (Sheet 1 of 2)

Memory Configuration	Power Domain	Decoupling Location	Qty x µF (size)	Note
DDR4 2 Channels SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10µF (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1µF (0402)	
		1 placeholder	1x 330µF (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Placeholder Place these caps on the VTT plane close to SODIMM	1x 10µF (0603)	
		Place these caps on the VTT plane close to SODIMM	4x 1µF (0402)	
	VPP	DIMM Side	2x 10µF (0603)	
		DIMM Side	2x 1µF (0402)	
	VDDSPD	Place close to DIMM	2x 0.1µF (0402)	
		Place close to DIMM	2x 2.2µF (0402)	

AVC	Asia Vital Components Co., Ltd.		
Title	P15 DDR4 CHA SO-DIMM2-8H		
Size C	Document Number A560-27IOB		Rev X03
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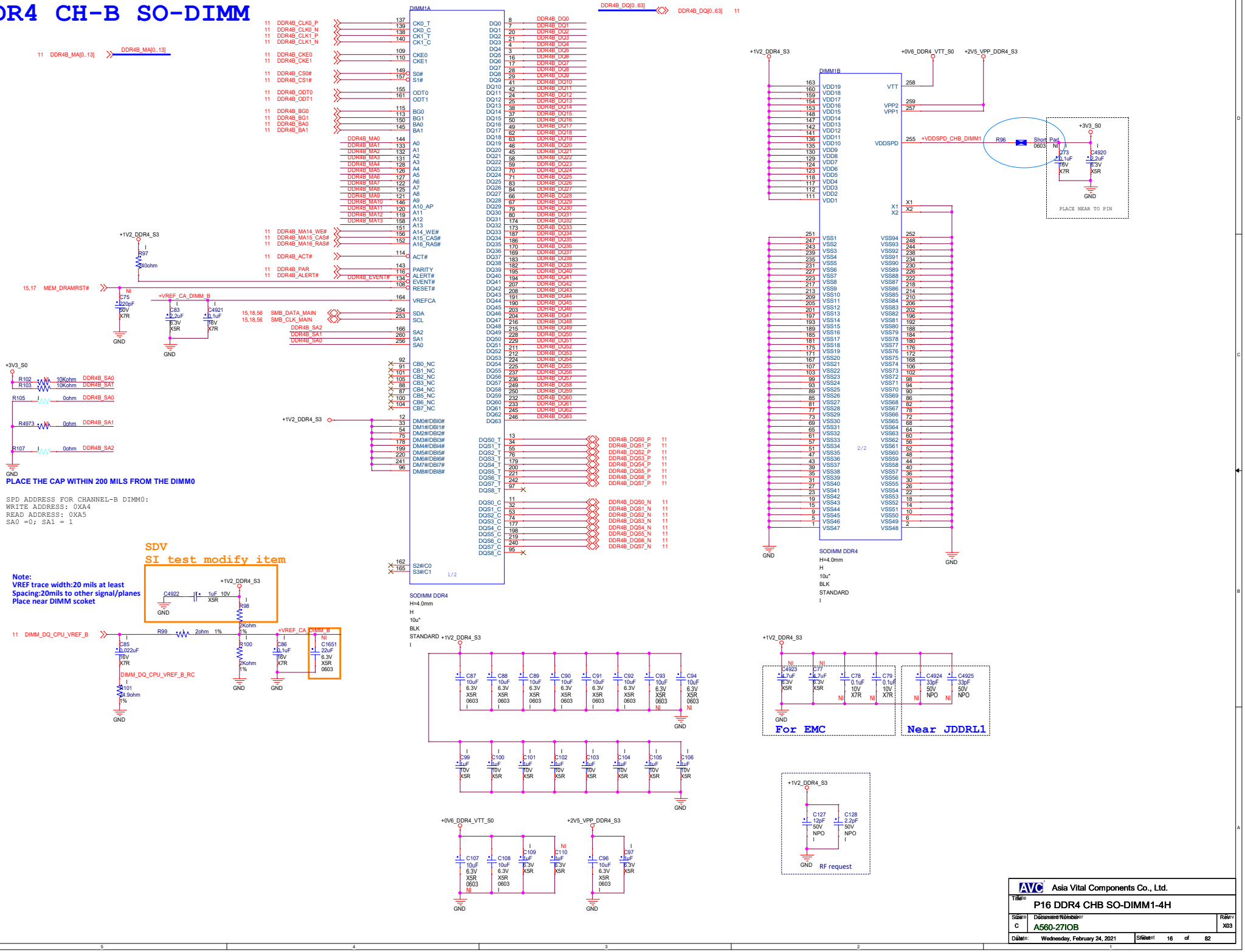
DDR4 CH-B SO-DIMM



Title	P16 DDR4 CHB SO-DIMM1-4H
Size	C
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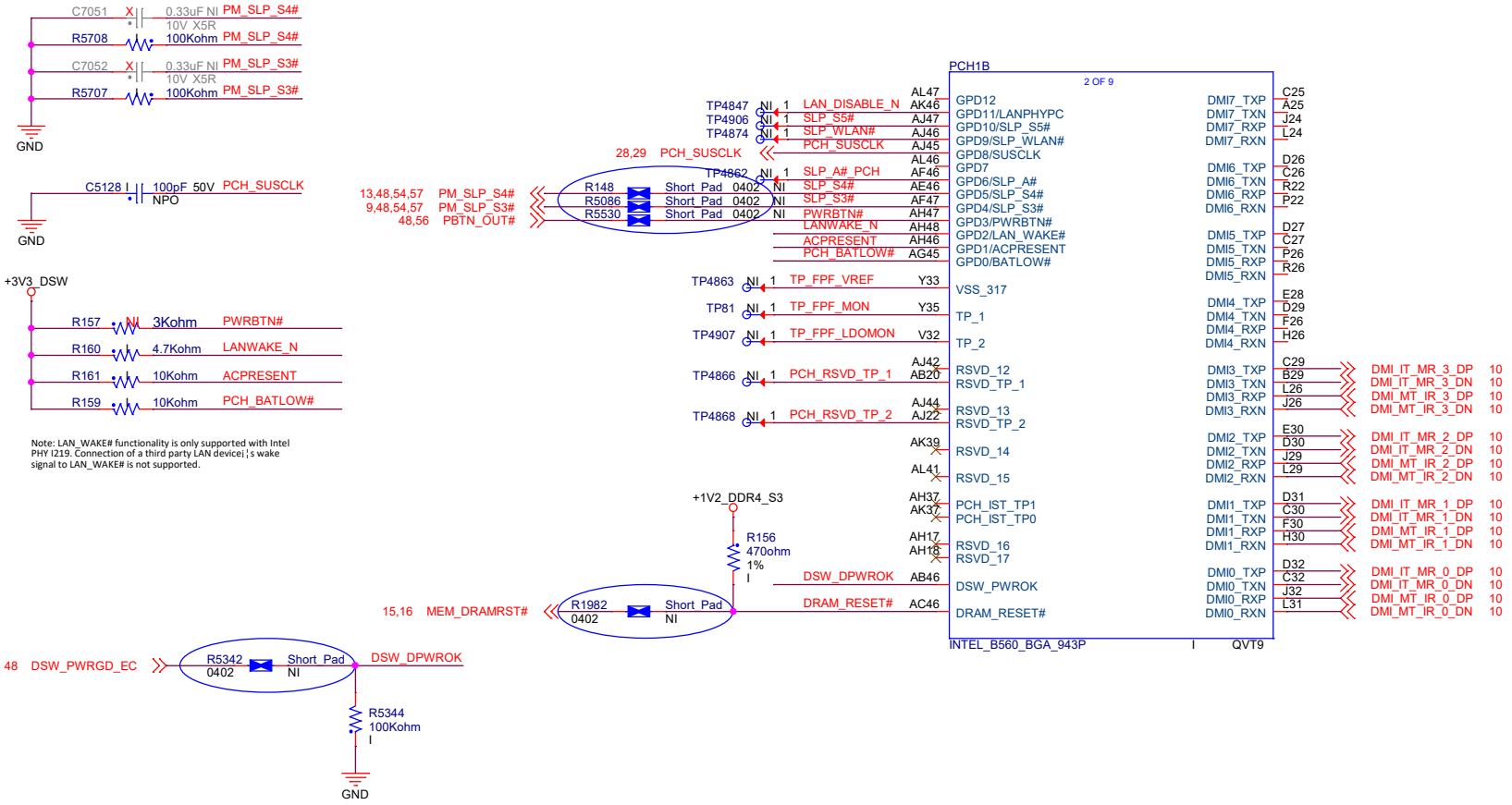
Asia Vital Components Co., Ltd.



Asia Vital Components Co., Ltd.			
Title: P17 PCH - DMI, SEQ SIGNAL			
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BOARD ID

BOARD ID MAP	ID5	ID4	ID3	ID2	ID1	ID0
A550 W/O GPU					0	
A550 W/GPU					1	
A550 24IMB						0
A550 27IMB						1

+1V8_S5 R5725 10Kohm NI BRD_ID5
R5724 10Kohm NI BRD_ID4
R5723 10Kohm NI BRD_ID3
R5655 10Kohm NI BRD_ID2
R131 10Kohm I BRD_ID1
R4985 10Kohm BRD_ID0
R133 NI 10Kohm
R134 10Kohm NI
R5654 10Kohm I
R5726 10Kohm I
R5727 10Kohm I
R5728 10Kohm I
GND

PCH1D
4 OF 9

48,55 BRD_ID1
BRD_ID0 AU29 GPP_D23/UART3_CTS#/THC1_SPI2_INT#
BRD_ID1 AY30 GPP_D22/UART3_RTS#/THC1_SPI2_RST#
BRD_ID2 AW29 GPP_D21/UART3_TXD/THC1_SPI2_IO3
BRD_ID3 BD30 GPP_D20/UART3_RXD/THC1_SPI2_IO2
BRD_ID4 BD35 GPP_D19/GSPI3_MOSI/THC1_SPI2_IO1
BRD_ID5 BD34 GPP_D18/GSPI3_MISO/THC1_SPI2_IO0
BE34 GPP_D17/GSPI3_CLK/THC1_SPI2_CLK
BE35 GPP_D16/GSPI3_CS0#/THC1_SPI2_CS#
BB30 GPP_D15/SML1DATA
BC30 GPP_D14/THC0_SPI1_IO3
BE30 GPP_D13/THC0_SPI1_IO2
BD31 GPP_D12/ISH_UART0_CTS#
BD32 GPP_D11
BC35 GPP_D10/SML0DATA
BE32 GPP_D9/SML0CLK
BD36 GPP_D8/I2S2_SCLK/THC0_SPI1_INT#
BE36 GPP_D7/I2S2_RXD/THC0_SPI1_RST#
AY35 GPP_D6/I2S2_TXD/MODEM_CLKREQ
BA33 GPP_D5/I2S2_SFRM/CNV_RF_RESET#
BF33 GPP_D4/SML1CLK
BD33 GPP_D3/THC0_SPI1_IO0/SBK3/BK3
BE33 GPP_D2/THC0_SPI1_IO1/SBK2/BK2
AW32 GPP_D1/THC0_SPI1_CLK/SBK1/BK1
AU31 GPP_D0/THC0_SPI1_CS#/SBK0/BK0

TO EC
48 SML1_DATA
SML0_DATA
SML0_CLK
28 CNV_CLKREQ0 R4834 33ohm CNV_CLKREQ0_R
28 CNV_RF_RST# R4833 33ohm CNV_RF_RST#_R
48 SML1_CLK
TO EC

48 SIO_SCI_N
BB26 GPP_C23/UART2_CTS#
AU26 GPP_C22/UART2_RTS#
AW26 GPP_C21/UART2_TXD
AY26 GPP_C20/UART2_RXD
BD26 GPP_C19/I2C1_SCL
BE26 GPP_C18/I2C1_SDA
BD27 GPP_C17/I2C0_SCL
BC22 GPP_C16/I2C0_SDA
BE23 GPP_C15/UART1_CTS#/ISH_UART1_CTS#
BD24 GPP_C14/UART1_RTS#/ISH_UART1_RTS#
BD23 GPP_C13/UART1_TXD/ISH_UART1_TXD
BC26 GPP_C12/UART1_RXD/ISH_UART1_RXD
BD29 GPP_C11/UART0_CTS#
BF29 GPP_C10/UART0_RTS#
BE29 GPP_C9/UART0_TXD
BE27 GPP_C8/UART0_RXD
BB24 GPP_C7/ISH_I2C2_SCL/I2C3_SCL
AY24 GPP_C6/ISH_I2C2_SDA/I2C3_SDA/SBK4/BK4
BD27 GPP_C5/SML0ALERT#
BE25 GPP_C4/ISH_UART0_TXD/I2C2_SCL
BD26 GPP_C3/ISH_UART0_RXD/I2C2_SDA
BD25 GPP_C2/SMBALERT#
BE26 GPP_C1/SMBDATA
GPP_C0/SMBCLK

55 DGPU_HOLD_RST#
55 GPU_PWR_GOOD
55 GPU_GC6_WAKE
55 GPU_GC6_EVENT
45 SMBUS_ISP
CLEAR_CMOS_N
53,60 detect wireless
25 SML0ALERT# Starps
25 SMBALERT# Starps
45 SMB_DATA_RESUME
45 SMB_CLK_RESUME
25 SML1ALERT# Starps
25 PCH_STRAP_GPP_B22 Starps
25 LPSS_GSPI0_MOSI Starps
25,36,48 SPKR
SPKR
PLTRST_R_N
48,54 PM_SLP_S0#
R5529 I 0ohm SLP_S0#

BD42 GPP_B23/SML1ALERT#/PCHHOT#
AW41 GPP_B22/GSPI1_MOSI
BE42 GPP_B21/GSPI1_MISO
BB42 GPP_B20/GSPI1_CLK
BD40 GPP_B19/GSPI1_CS0#
AU36 GPP_B18/GSPI0_MOSI
BA36 GPP_B17/GSPI0_MISO
AY36 GPP_B16/GSPI0_CLK
BA35 GPP_B15/GSPI0_CS0#
BD40 GPP_B14/SPKR
BD39 GPP_B13/PLTRST#
BE40 GPP_B12/SLP_S0#
BE39 GPP_B11/I2S_MCLK
BD38 GPP_B10/SRCCLKREQ5#
BE38 GPP_B9/SRCCLKREQ4#
BF37 GPP_B8/SRCCLKREQ3#
BD37 GPP_B7/SRCCLKREQ2#
BC38 GPP_B6/SRCCLKREQ1#
BC37 GPP_B5/SRCCLKREQ0#
AU34 GPP_B4/CPU_GP3
AW35 GPP_B3/CPU_GP2
AY33 GPP_B2/VRALERT#
AY34 GPP_B1/GSPI1_CS1#/TIME_SYNC1
AW37 GPP_B0/GSPI0_CS1#/IMGCLKOUT1

28 CLK_REQ3_M.2_WLAN#
29 CLK_REQ2_M.2_SSD#
30 CLK_REQ1_LAN#
55 CLK_REQ0_DGPU#
48 EC_SCI#
28 M.2_BT_DISABLE_N

INTEL_B560_BGA_943P
QVT9

GPP_A14/IMGCLKOUT0 AW46
GPP_A13/ESPI_ALERT3# AV46
GPP_A12/ESPI_ALERT2# AV47
GPP_A11/ESPI_ALERT1# AU45
GPP_A10/ESPI_ALERT0# AU46 ESPI_ALERT0# 48
GPP_A9/ESPI_CS3# AU47
GPP_A8/ESPI_CS2# AT48
GPP_A7/ESPI_CS1# AT46
ESPI_RESET# AT45
GPP_A6/ESPI_RESET# AR47 PCH_ESPI_CLK R123 33ohm 1% ESPI_RESET# 48 EC_ESPI_CLK 48
GPP_A5/ESPI_CLK AR46 ESPI_CS# ESPI_CS# 48
GPP_A4/ESPI_CS0# AP46 PCH_ESPI_IO3 R4760 33ohm 1% EC_ESPI_IO3 48
GPP_A3/ESPI_IO3/SUSACK# AP47 PCH_ESPI_IO2 R4761 33ohm 1% EC_ESPI_IO2 48
GPP_A2/ESPI_IO2/SUSWARN#/SUSPWRDNACK AN45 PCH_ESPI_IO1 R4762 33ohm 1% EC_ESPI_IO1 48
GPP_A1/ESPI_IO1 AN46 PCH_ESPI_IO0 R4763 33ohm 1% EC_ESPI_IO0 48
GPP_A0/ESPI_IO0

Close to PCH

GPP_G15/DDP2_CTRLDATA/TBT_LSX1_RXD AL21
GPP_G14/DDP2_CTRLCLK/TBT_LSX1_TXD AN21
GPP_G13/DDP1_CTRLDATA/TBT_LSX0_RXD AU19
GPP_G12/DDP1_CTRLCLK/TBT_LSX0_TXD AW18
GPP_G11/ISH_SPI_MOSI/DDP4_CTRLDATA/GSPI2_MOSI/TBT_LSX3_RXD AY17
GPP_G10/ISH_SPI_MISO/DDP4_CTRLCLK/GSPI2_MISO/TBT_LSX3_TXD BA17
GPP_G9/ISH_SPI_CLK/DDP3_CTRLDATA/GSPI2_CLK/TBT_LSX2_RXD BC17
GPP_G8/ISH_SPI_CS#/DDP3_CTRLCLK/GSPI2_CS0#/TBT_LSX2_TXD BE18

GPP_G7 BF17 TPM_SEL R2092 I 0ohm TPM_SELECT 51
GPP_G6 BD17 SPI_TPM_PIRQ 51
GPP_G5/SLP_DRAM# BE17
GPP_G4 BD16
GPP_G3 BD20
GPP_G2/DNX_FORCE_RELOAD BE15 TP_DNX_FORCE_RELOAD 1 NI TP4869
GPP_G1/DDPA_CTRLDATA BD15
GPP_G0/DDPA_CTRLCLK BD14

GPP_RCOMP BG13 GPP_RCOMP R5065 200ohm 1% GND
PCIE_RCOMPP B13 PCIE_RCOMPP
PCIE_RCOMPN A13 PCIE_RCOMPN R214 100ohm 1%

CL_RST# AR3 CLINK_RST# 28
CL_DATA AR4 CLINK_CLK 28
CL_CLK AP4 CLINK_DATA 28

PCH_JTAGX AM2 CPU_H_TCK 9,56
PCH_JTAG_TMS AM4 CPU_H_TMS 9,56
PCH_JTAG_TDO AM3 CPU_H_TDO 9,56
PCH_JTAG_TDI AN4 CPU_H_TDI 9,56
PCH_JTAG_TCK AM5 PCH_TCK 56

DBG_PMODE AG5 ITP_PMODE 56
INTRUDER# AE47 PCH_INTRUDER#

HDACPU_SDO AJ5 HDACPU_SDO R162 22ohm PROC_AUDIO_SDI 10
HDACPU_SDI AK4 HDACPU_SDI HDACPU_SDI 10
HDACPU_BCLK AJ3 HDACPU_BCLK R163 22ohm PROC_AUDIO_CLK 10
close to PCH

+1V8_S5
R173 1Kohm SML1_CLK
R174 1Kohm SML1_DATA
R169 1Kohm SML0_CLK
R171 1Kohm SML0_DATA

R5412 10Kohm DGPU_HOLD_RST#
Close to PCH
GND

+3V3_S5
R2089 10Kohm I GPU_GC6_WAKE
R5532 10Kohm NI
GND

+3V3_S5
R2373 10Kohm CLK_REQ3_M.2_WLAN#
R5095 10Kohm CLK_REQ2_M.2_SSD#
R2374 10Kohm CLK_REQ1_LAN#
R1921 10Kohm CLK_REQ0_DGPU#
Close to Device

ESPI_RESET#
ESPI_CS#
R5060 75Kohm I GND
R5023 75Kohm I GND

+3V3_S5
TPM_SEL R208 10Kohm
SPI_TPM_PIRQ R5605 10Kohm

SDV
R165 change to NI
ITP_PMODE R165 NI 1Kohm GND

+3V3_VBAT
PCH_INTRUDER# R187 1Mohm 1%
C4945 X NI 0.1uF 10V X7R GND

SDV
SI solution
+VCCSTG
CPU_H_TDO R5353 NI 100ohm 1%
CPU_H_TDI R5354 51ohm
CPU_H_TMS R5698 51ohm
CPU_H_TCK R5677 NI 51ohm
close to PCH
GND

+3V3_S5
C1704 0.1uF 10V X7R NI GND
U134 SN74LVC1G08DBVR NI
PLTRST_N
U134_4
R5697 0402 Short_Pad NI
PCH_PLTRST_N 28,29,30,48,51,55,56
C5534 330pF 50V X7R I GND
PLTRST_R_N
R2364 0402 Short_Pad NI
R193 0402 Short_Pad NI

SMB RESUME/MAIN LOGIC

+3V3_S5
R2024 2.2Kohm
R2025 2.2Kohm
Q185A 50V 0.2A 5V@3.5ohm LBSS138DW1T1G
SMB_CLK_RESUME
SMB_CLK_MAIN 15,16,56
+3V3_S0
R2026 2.2Kohm
R2027 2.2Kohm
Q185B 50V 0.2A 5V@3.5ohm LBSS138DW1T1G
SMB_DATA_RESUME
SMB_DATA_MAIN 15,16,56
+3V3_S0

CLEAR CMOS
+3V3_S5
R229 10Kohm
CLEAR_CMOS_N
C_CMOS
C_CMOS1
GND
1-2 : DEFAULT
2-3 : CLEAR CMOS

	V	GF	RED	1x3P	2.54mm
JUMPER	GF	RED	Open	1x2P	2.54mm

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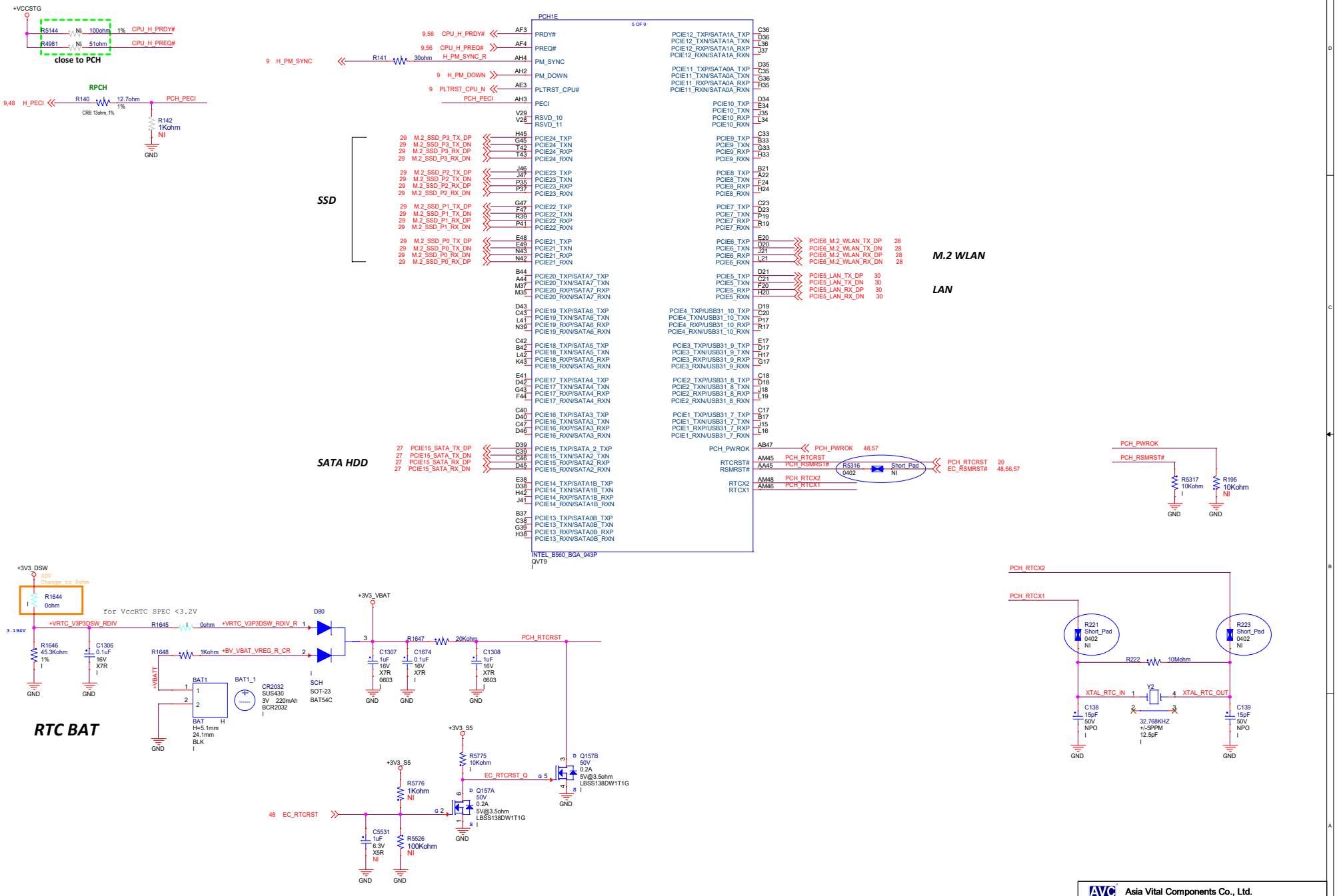
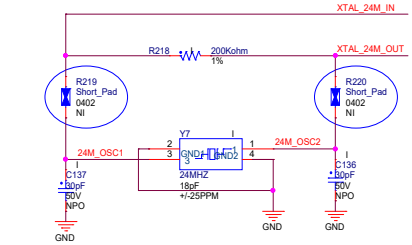
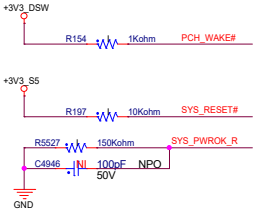
Asia Vital Components Co., Ltd.
Title: P18 PCH - eSPI, SMB, CLKREQ
Size: C
Document Number: A560-27IOB
Rev: X03
Date: Wednesday, February 24, 2021
Sheet 18 of 82

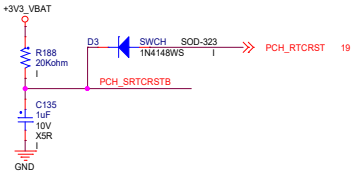


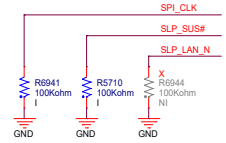
AVC Asia Vital Components Co., Ltd.			
Title: P19 PCH - PCIE			
Size: C	Document Number: A560-27IOB		Rev: X03
Date: Wednesday, February 24, 2021	Sheet 19 of 82		

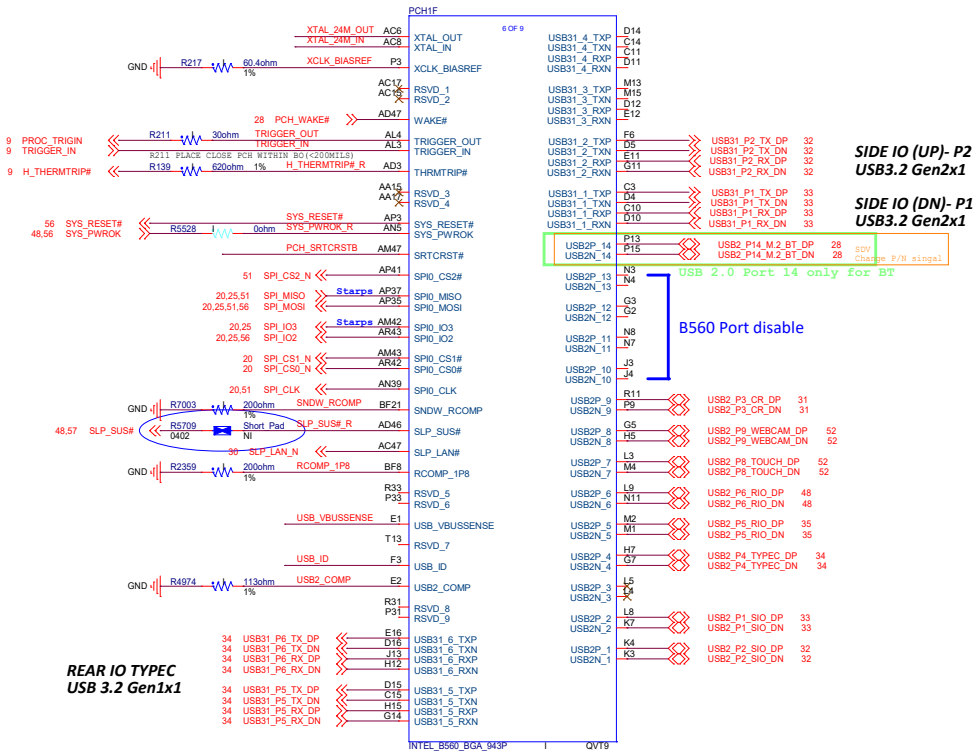
PCH - USB / SPI





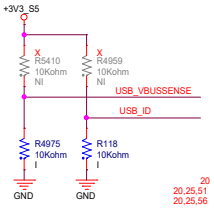


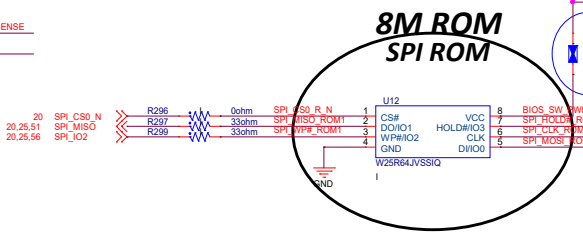


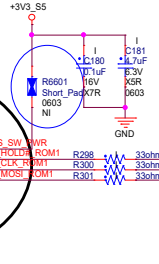


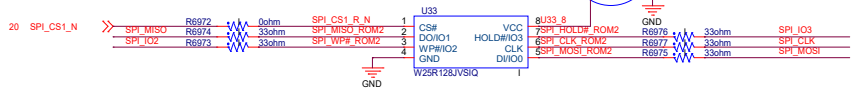
REAR IO TYPEC
USB 3.2 Gen1x1

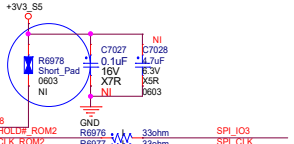
USB2 Port	IO FUNCTION	OC No.
PORT 1	SIDE IO (UP) - P2: USB3.1 Gen1	OC0
PORT 2	SIDE IO (DN) - P1: USB3.1 Gen1	OC0
PORT 3		
PORT 4	REAR IO - P3,4: USB3.1 Gen1	OC1
PORT 5	REAR IO - : USB2.0	OC2
PORT 6	REAR IO - : USB2.0 Smart PWR on	OC2
PORT 7	TOUCH	OC3
PORT 8	CAMERA	
PORT 9	CARD READER	
PORT 10	Port disable	
PORT 11	Port disable	
PORT 12	Port disable	
PORT 13	Port disable	
PORT 14	M.2 BT	

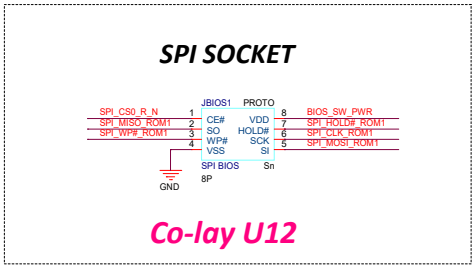


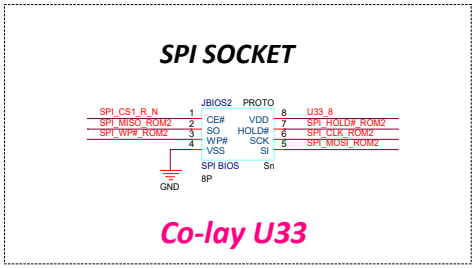




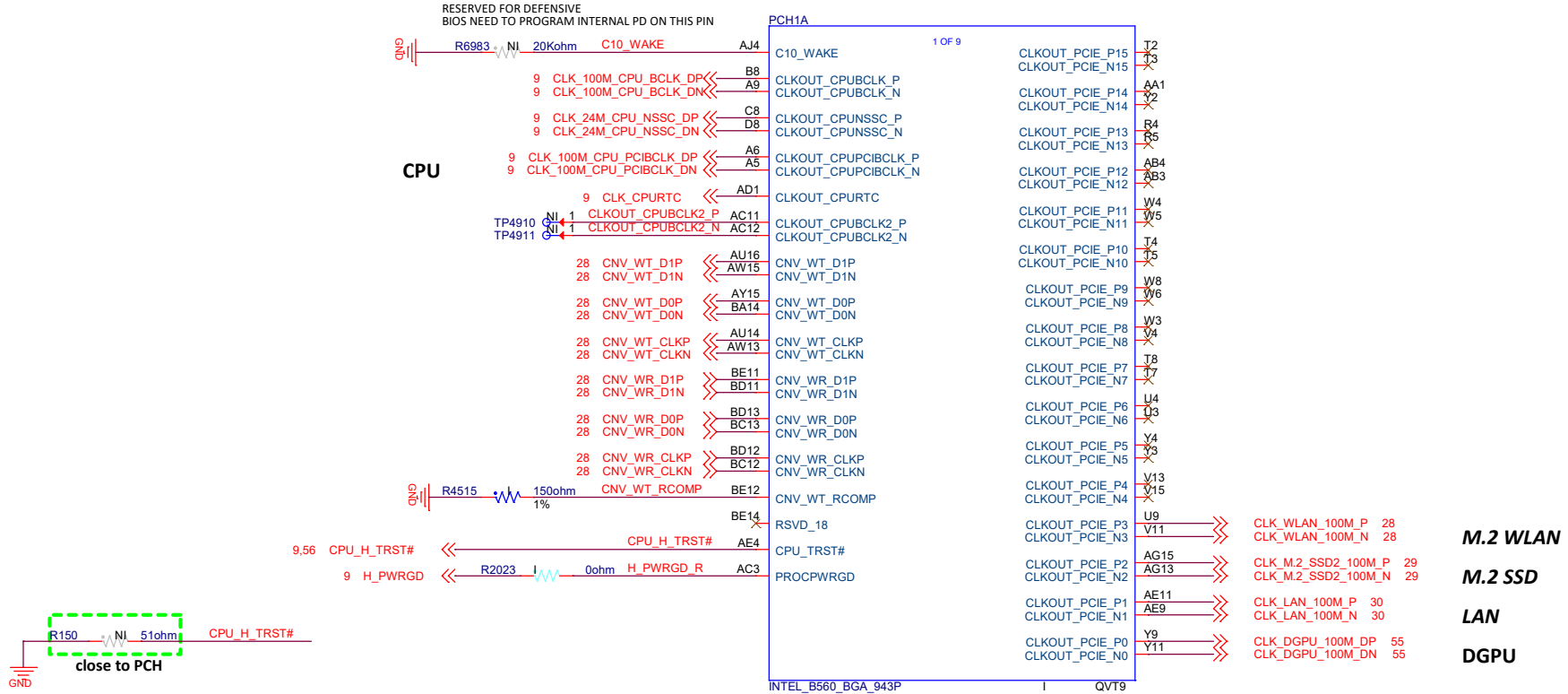








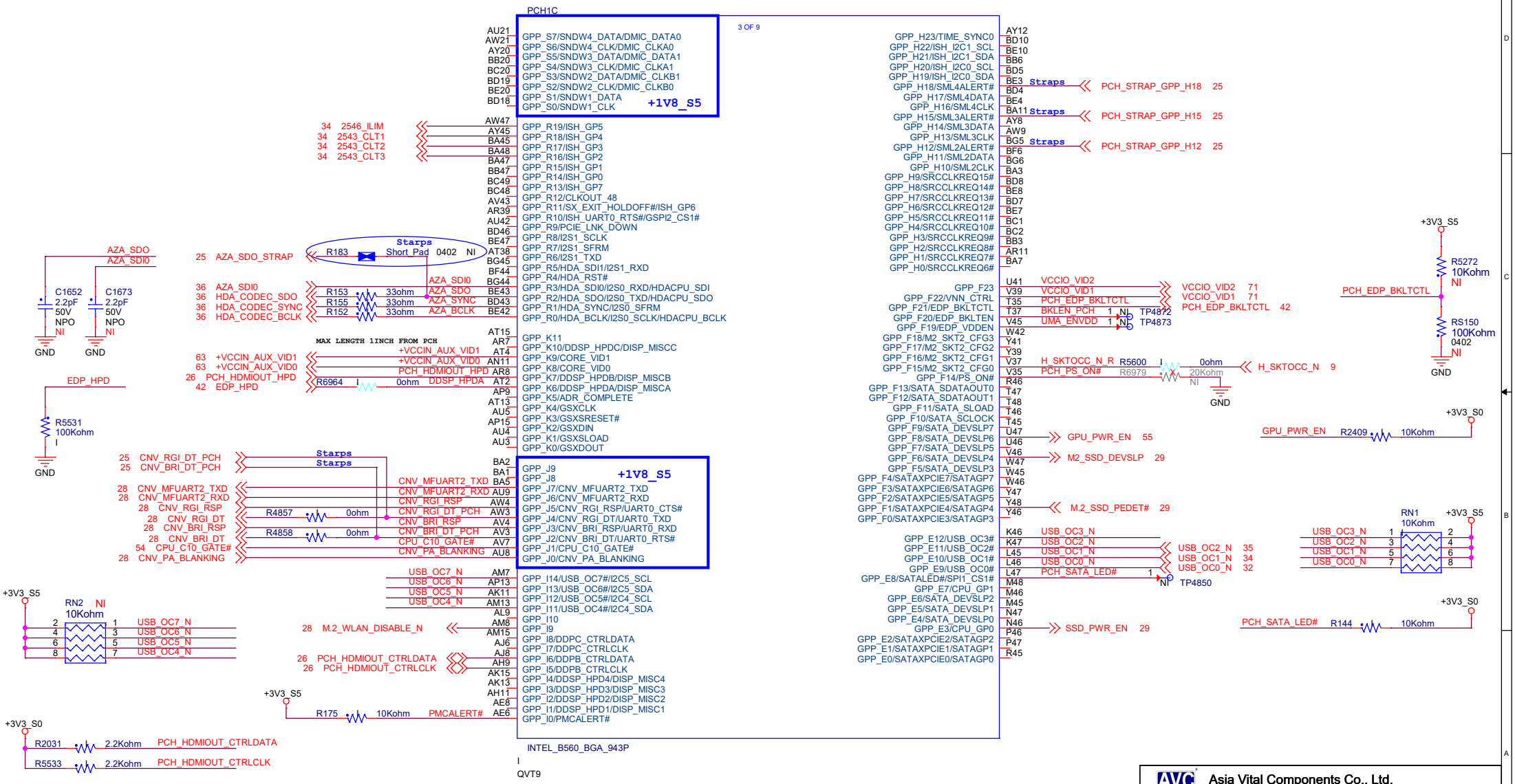
AVC	Asia Vital Components Co., Ltd.		
Title	P20 PCH - USB, SPI		
Size C	Document Number A560-27IOB		Rev X03
Date:	Wednesday, February 24, 2021	Sheet 20 of 82	



Name	Type	SSC Capable	Description
CLKOUT_PCIE_P[15:0] CLKOUT_PCIE_N[15:0]	O	Yes	**PCI Express* Clock Output:** Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices • CLKOUT_PCIE_P/N [15:0] = Can be used for PCIe* Gen1/2/3 support • CLKOUT_PCIE_P/N [9, 7, 4, 3, 0] = Must be used for PCIe* Gen4 support

AVC Asia Vital Components Co., Ltd.			
Title: P21 PCH - CLK, CNVi			
Size: B	Document Number: A560-27IOB		Rev: X03
Date: Wednesday, February 24, 2021	Sheet 21 of 82		

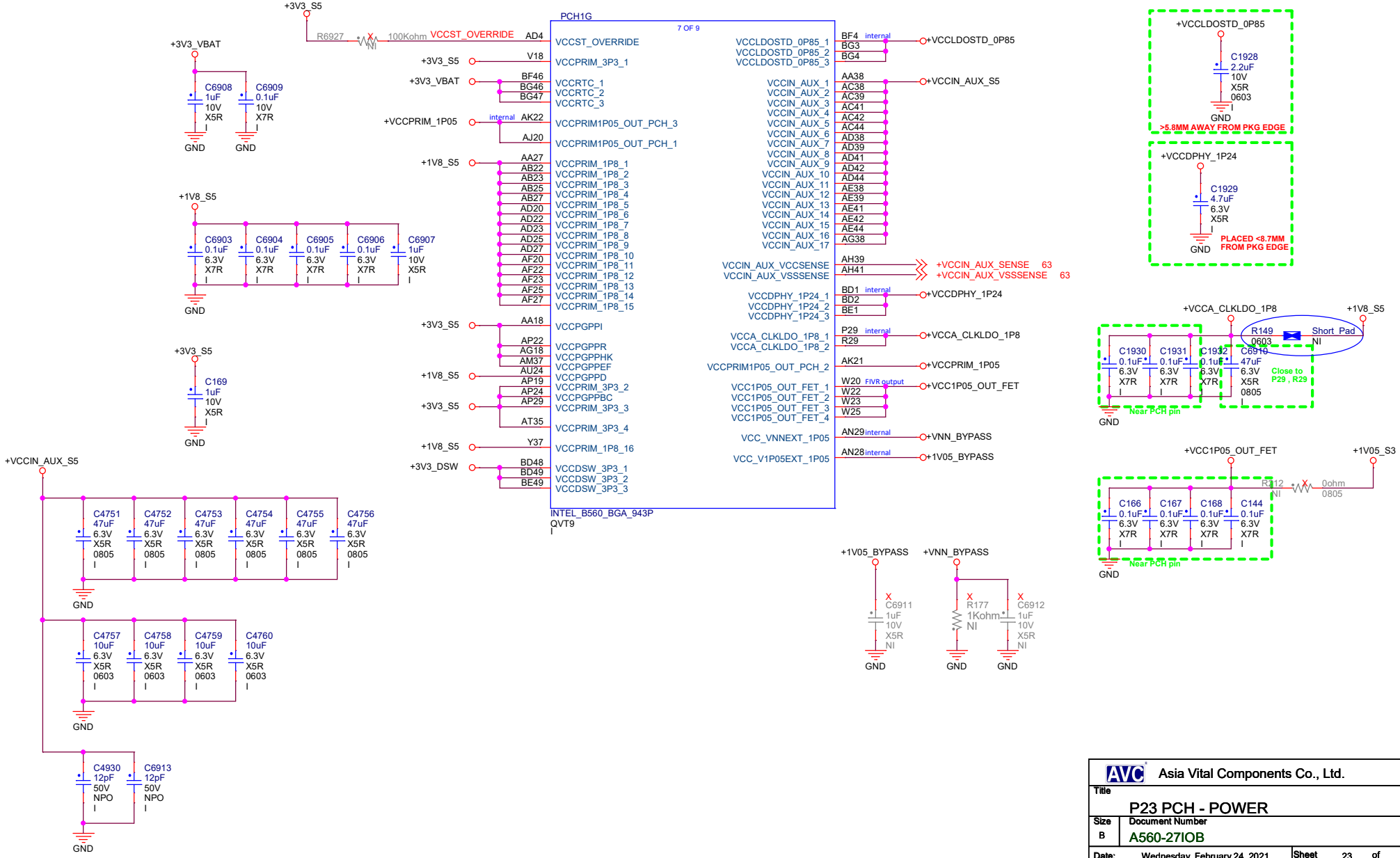
PCH - HDA, HPD, USB_OC



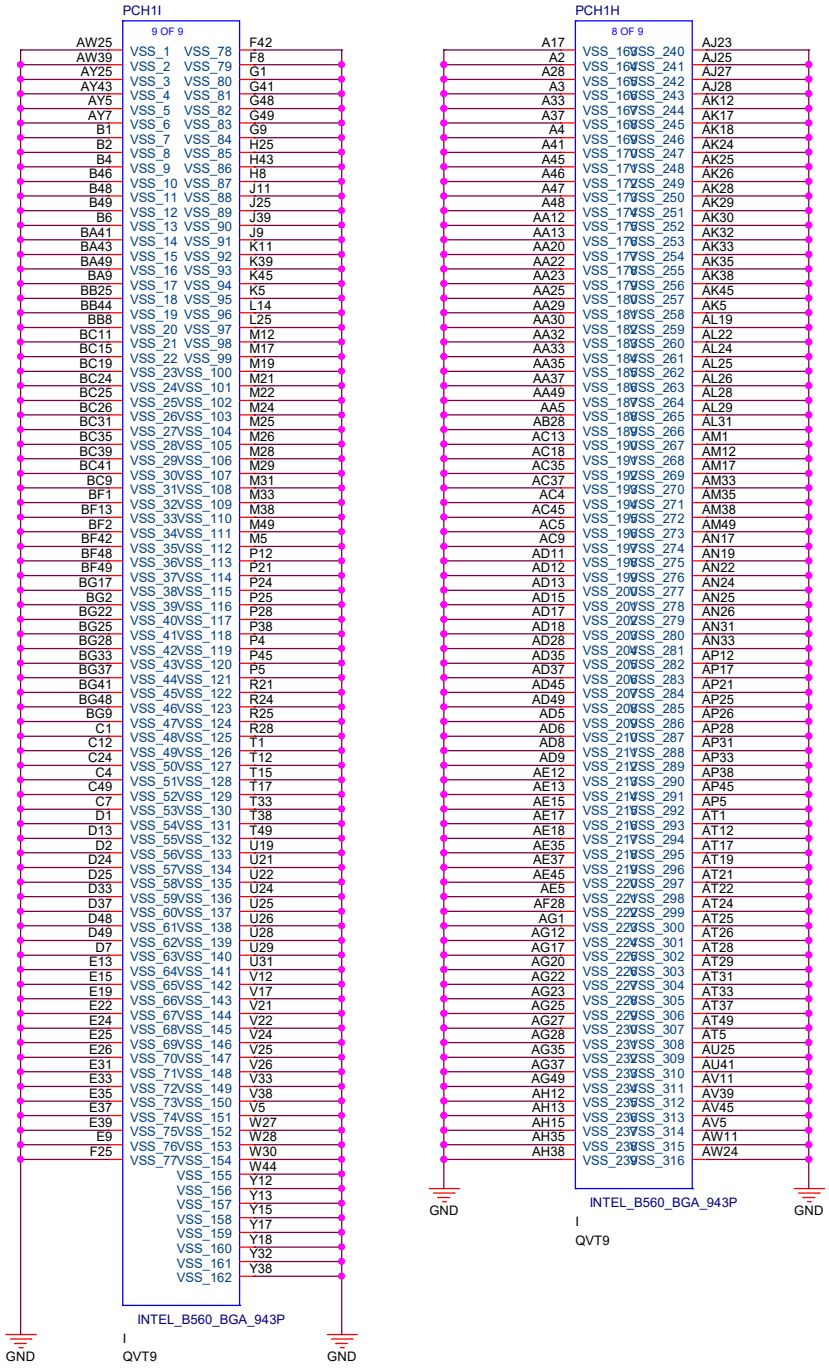
AVC Asia Vital Components Co., Ltd.			
Title: P22 PCH - HDA, HPD, USB_OC			
Size: B	Document Number: A560-27IOB		Rev: X03
Date: Wednesday, February 24, 2021	Sheet 22 of 82		

PCH POWER

VCCST_OVERRIDE	O	**VccST Override:** Signal that allows the PCH to keep VCCST powered ON (in case VCCST is powered down) for USB-C wake capability. Signal will stay high when plug-in device on TCSS port and signal will stay low when no device is connected.



AVC Asia Vital Components Co., Ltd.			
Title: P23 PCH - POWER			
Size: B	Document Number: A560-27IOB		Rev: X03
Date: Wednesday, February 24, 2021	Sheet 23 of 82		

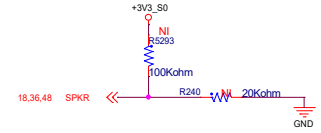


AVC Asia Vital Components Co., Ltd.		
Title: P24 PCH - GND		
Size: B	Document Number: A560-27IOB	Rev: X03
Date: Wednesday, February 24, 2021	Sheet 24 of 82	

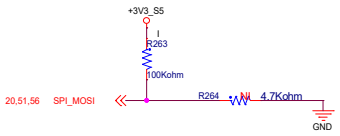
PCH STRAPS

GPP_B14 / SPKR

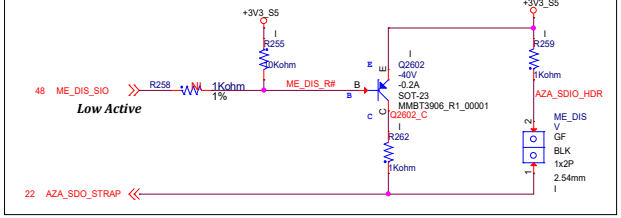
TOP SWAP OVERRIDE STRAP
1: TOP SWAP ENABLED
0: TOP SWAP DISABLED (DEFAULT)
PCH HAS INTERNAL WEAK PD



BOOT HALT ENABLED IF LOW
PCH HAS INTERNAL WEAK PU

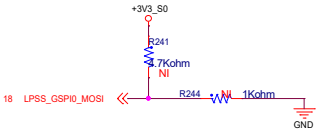


HDA_SDO / I2S0_TXD
Flash Descriptor Security Override
0 = Enable security measures defined in the Flash Descriptor. (Default)
1 = Disable Flash Descriptor Security (override).
PCH has a weak internal pull-down.

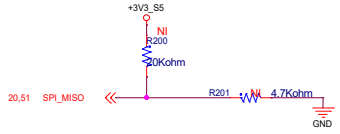


GPP_B18 / GSPI0_MOSI

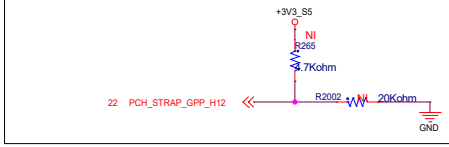
0 = Disable ¡§No Reboot¡¨ mode. (Default)
1 = Enable ¡§No Reboot¡¨ mode
NO REBOOT IF SAMPLED HIGH
PCH HAS INTERNAL WEAK PD



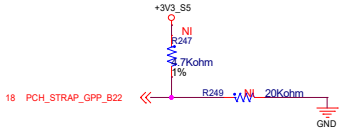
JTAG ODT IS DISABLED IF LOW
PCH HAS INTERNAL WEAK PU



GPP_H12 / SML2ALERT#
ESPI FLASH SHARING MODE
0: MASTER ATTACHED FLASH SHARING
1: SLAVE ATTACHED FLASH SHARING
PCH HAS INTERNAL WEAK PD

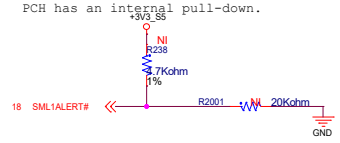


GPP_B22 / GSPI1_MOSI
TLS CONFIDENTIALITY ENABLED
PCH HAS INTERNAL WEAK PD
IF SAMPLED HIGH(DEFAULT)

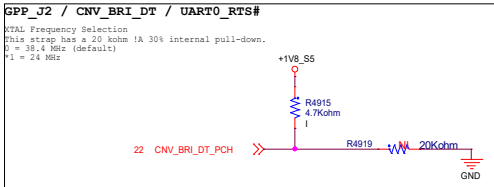


GPP_B23 / SML1ALERT# / PCHHOT#

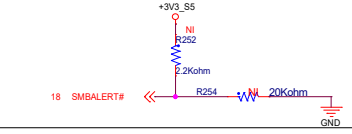
Intel DCI-OOB
0 = Disable Intel DCI-OOB (Default)
1 = Enable Intel DCI-OOB
PCH has an internal pull-down.



GPP_J2 / CNV_BRI_DT / UART0_RTS#
XTAL Frequency Selection
This strap has a 20 kohm !A 30% internal pull-down.
0 = 38.4 MHz (default)
*1 = 24 MHz

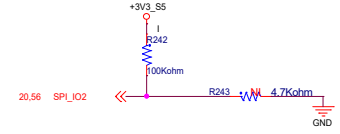


GPP_C2 / SMBALERT#
This signal has a weak internal Pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).

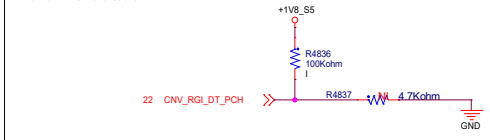


SPI0_IO2

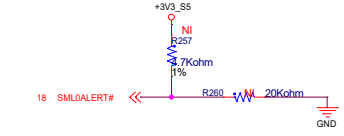
Reserved
CONSENT STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU



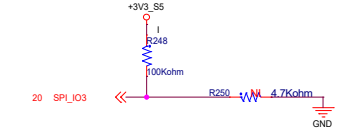
GPP_J4 / CNV_RGI_DT / UART0_TXD
CNVi mode select
This strap does not have an internal pull-up or pull-down. A weak external pull-up is required.
0=>M.2 CNVI MODES enable
*1=>M.2 CNVI MODES disable



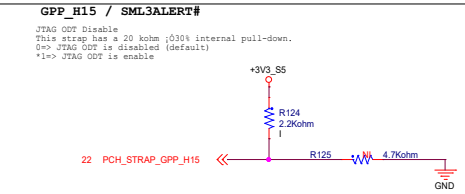
GPP_C5 / SML0ALERT#
ESPI/LPC SELECT STRAP
IF SAMPLED HIGH, ESPI IS SELECTED ELSE LPC
PCH HAS INTERNAL WEAK PD



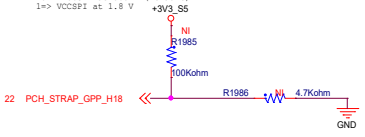
SPI0_IO3
Reserved
PESONALITY STRAP IS ENABLED IF LOW
PCH HAS INTERNAL WEAK PU



GPP_H15 / SML3ALERT#
JTAG ODT Disable
This strap has a 20 kohm ¡Ó30% internal pull-down.
0=> JTAG ODT is disabled (default)
*1=> JTAG ODT is enable



GPP_H18 / SML4ALERT#
VCCSPI Voltage Configuration
This strap has a 20 kohm ¡Ó30% internal pull-down.
*0=> VCCSPI at 3.3 V (Default)
1=> VCCSPI at 1.8 V



AVC Asia Vital Components Co., Ltd.		
Title: P25 PCH Straps		
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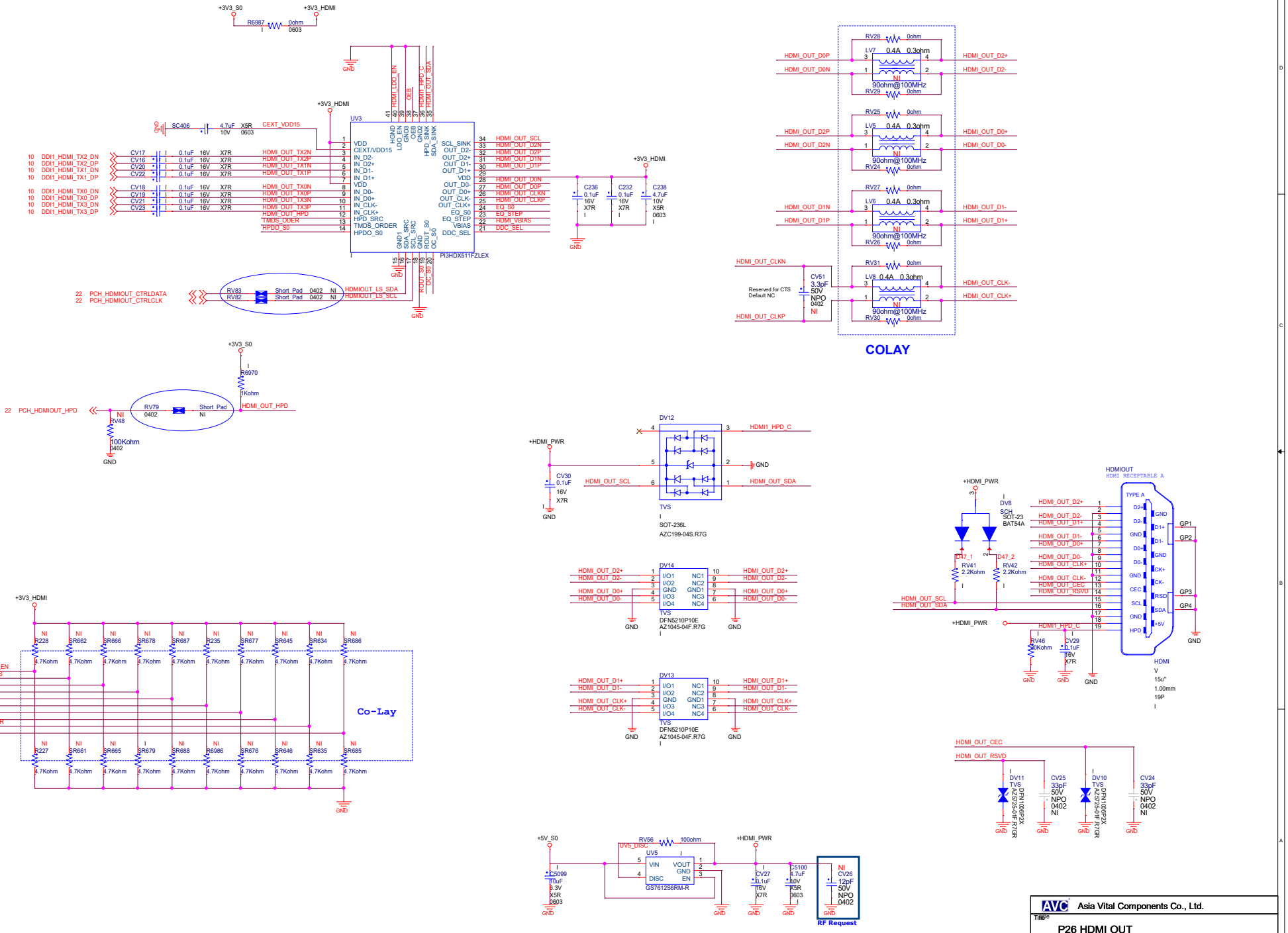
HDMI OUT



Asia Vital Components Co., Ltd.			
Title: P26 HDMI OUT			
Size: C	Document Number: A560-27IOB		Rev: X03
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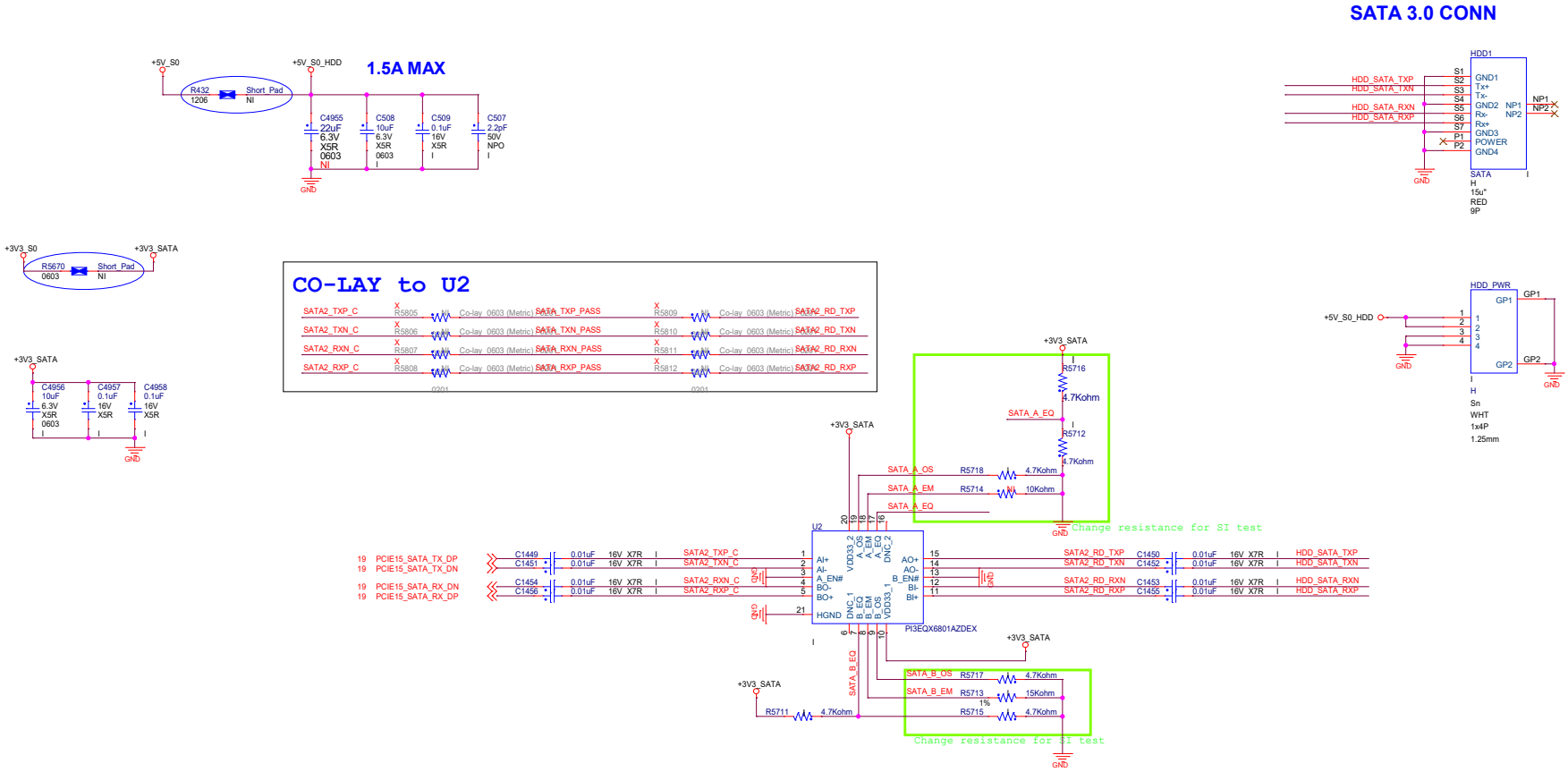
2.5" HDD



Receive Equalizer Configuration Table

x_EN#	x_EQ	Input Equalization @ 3.0GHz	Function
1	X	N/A	Channel x disabled. Hi-impedance terminations
0	0	8dB	Channel enabled, medium input equalization
0	1	16dB	Channel enabled, high input equalization
0	$V_{DD}/2$	4dB (Default)	Channel enabled, low input equalization

Output Swing Adjustment (1)

R[A:B]_OS (Ω)	Output Swing, mV ($V_{TX-DIFF-P}$)(2)	
	3Gbps	6Gbps
5.5K	450	600
5K	490	660
4.5K	540	730
4K	600	820
3.5K	670	910
3K	760	1,000
2.5K	870	1,080
2K	990	1,200

Note:
1. Suggested initial test values. Exact resistor values will vary depending on PCB design.
2. Auto HDD Rate Detection is ON.

Output Emphasis Adjustment (1, 2)

R[A:B]_EM (Ω)	Pre-emphasis
Do Not Connect	0dB
14K	+2.0dB
10K	+3.0dB
6K	+4.0dB
2K	+6.0dB

Note:
1. Suggested initial test values. Exact resistor values will vary depending on PCB design.
2. Referenced to output saving of 600mV, will vary as a function of swing, increasing as swing decreases.

Note:
V_{MAX} of output can not exceed 1,200mVppd (i.e. $V_{DIFF-PRE}$ can not exceed 1,200mV)

PIN CONFIGURATION for CONTROL

PIN NAME	PIN FUNCTION DESCRIPTION	Control Configuration
A_EN# B_EN#	With Internal 200k-ohm pull-down resistor Low: Normal Operation High: Power Down Mode	For real application, they could be OPEN.
A_EQ B_EQ	Input Equalization Tri-level Input	Equalization is controled by PIN7&PIN17 Input Equalization for Channel A&B: Input Equalization@3.0Gb/s: 0 = 8dB (A&B-CH); 1 = 16dB (A&B-CH); Vdd/2 = 4dB (A&B-CH)
A_EM B_EM	Output Emphasis Adjustment it is analog resistive adjustment. please refer to the next row table	Emphasis is controlled by PIN4&13, PIN5&12 and PIN6&11 of SW1 for Channel A, PIN4&13, PIN5&12 and PIN6&11 of SW2 for Channel B, Pre-emphasis for Channel A&B: PIN4&13 is Open = 0dB; PIN4&13 is short(14k RES) = +2.0dB; PIN5&12 is short(10k RES) = +3.0dB; PIN6&11 is short(6k RES) = +4.0dB
A_OS B_OS	Output Swing Adjustment it is analog resistive adjustment. please refer to the next row table	Swing is controlled by PIN1&16, PIN2&15 and PIN3&14 of SW1 for Channel A, PIN1&16, PIN2&15 and PIN3&14 of SW2 for Channel B, Swing Output for Channel A&B (mV, Vtx-diff-p at 6.0Gb/s): PIN1&16 is short(5k RES) = 660; PIN2&15 is short(4k RES) = 820; PIN3&14 is short(2k RES) = 1200
PIN6&16 PIN10&20	Voltage PIN	PI3EQX6801AZDE(3.3V)@TQFN20: PIN10&20=VDD33 (3.3V), PIN6&16=DNC

Asia Vital Components Co., Ltd.

Title	P27 SATA 3.0_Redriver	
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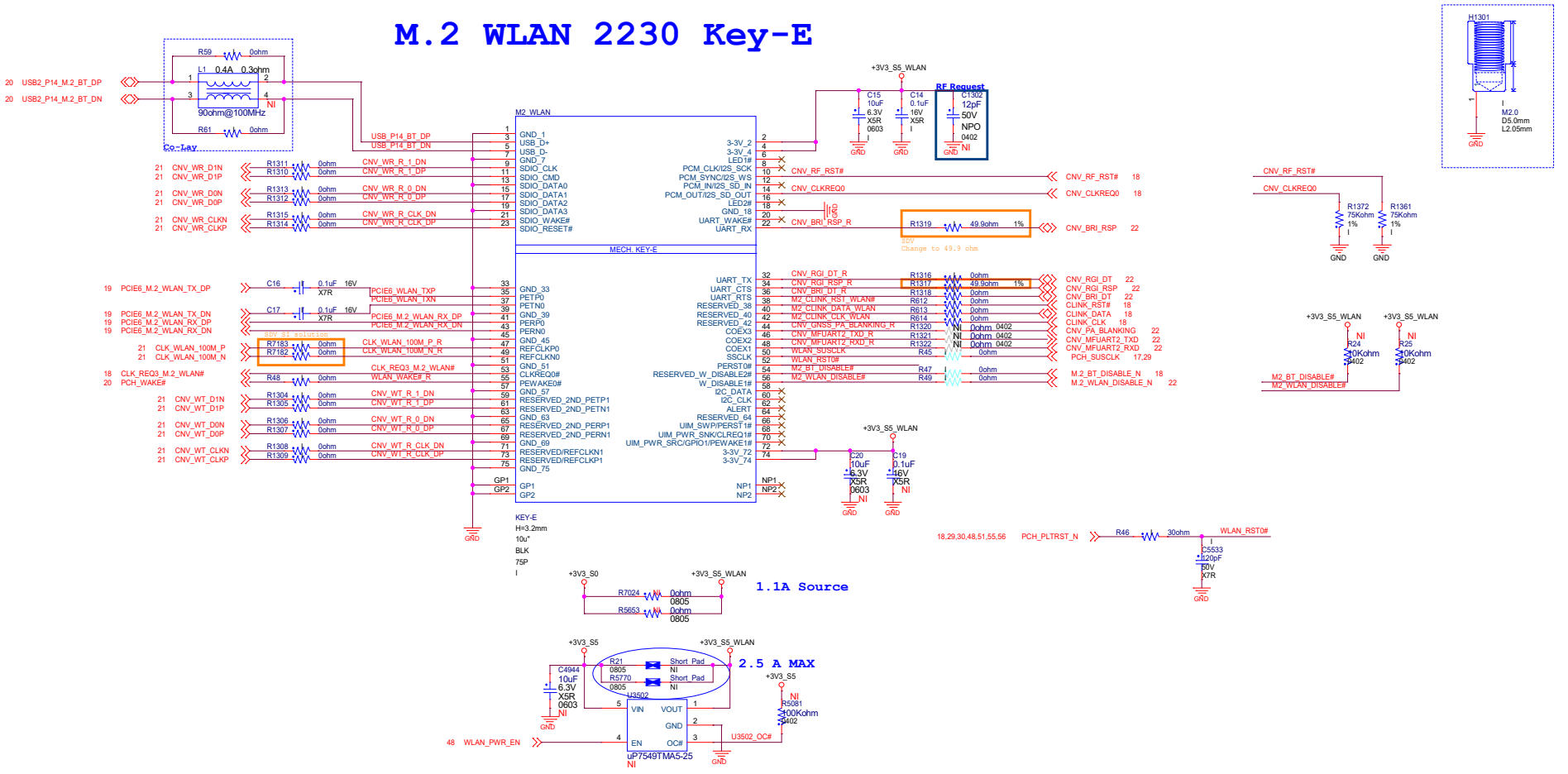
M.2 WLAN 2230 Key-E



Company	Asia Vital Components Co., Ltd.
Title	P28 M2 WLAN
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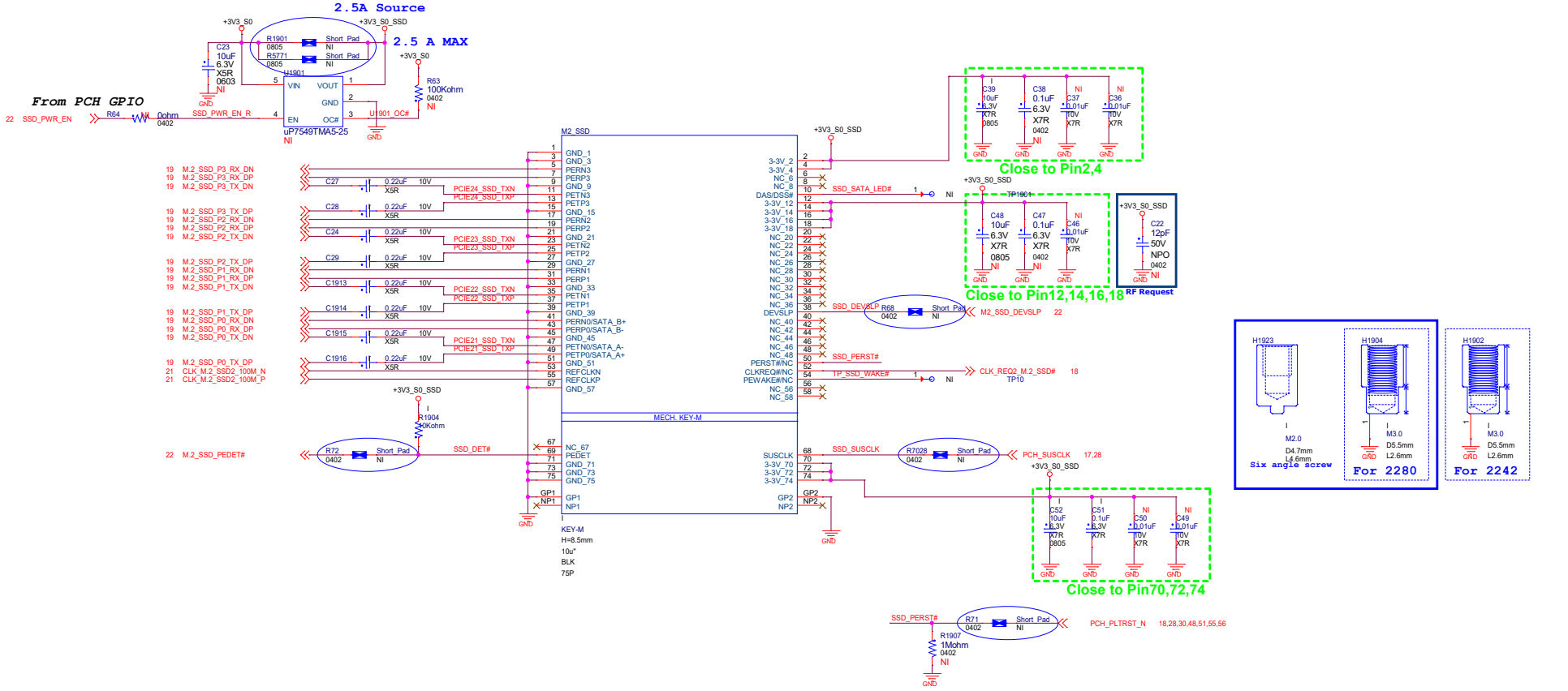
M.2 SSD 2242/ 2280



Asia Vital Components Co., Ltd.	
Title	P29 M2 SSD
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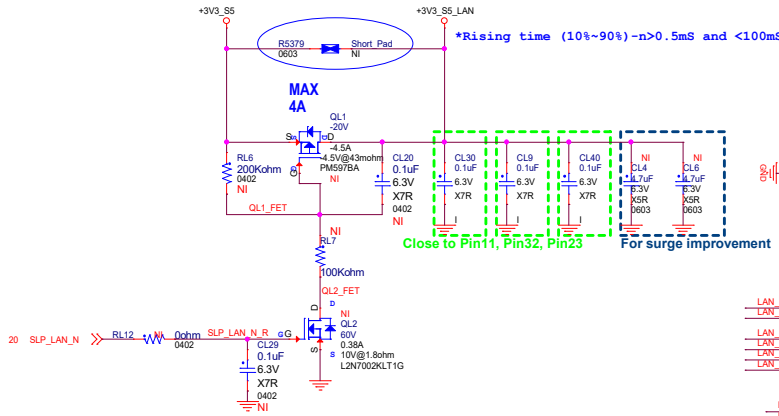
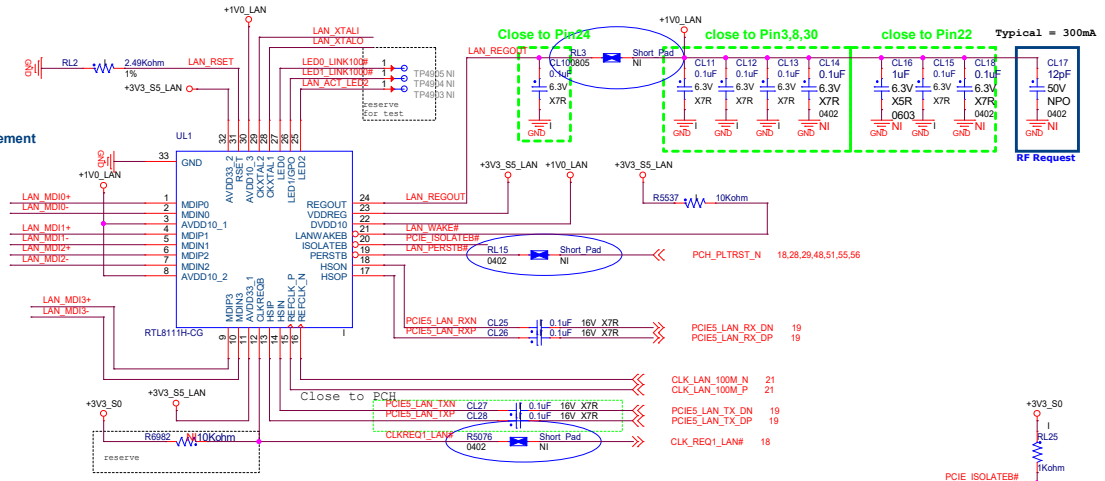
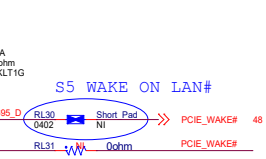
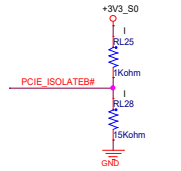
LAN RTL8111H-CG/ RJ45 CONN

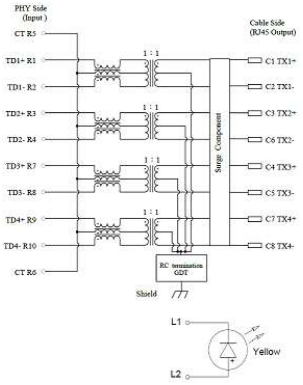


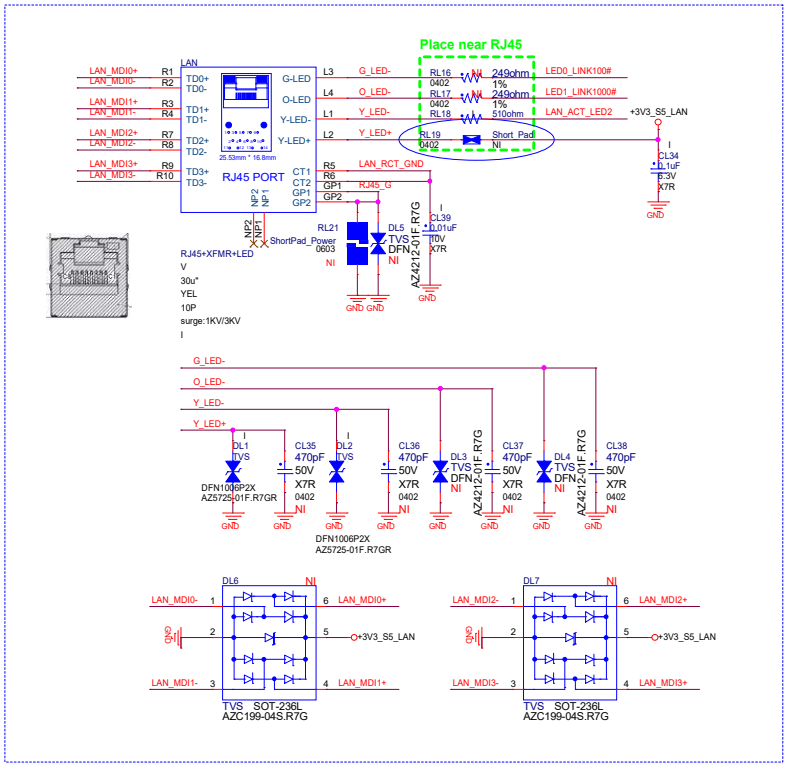


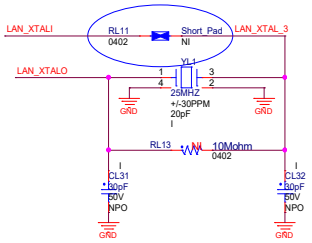




WOL	status	Yellow
don't care	No Link	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off
on	10M,inactive	
on	10M,active	
on	100M,inactive	
on	100M,active	
on	1G,inactive	
on	1G,active	







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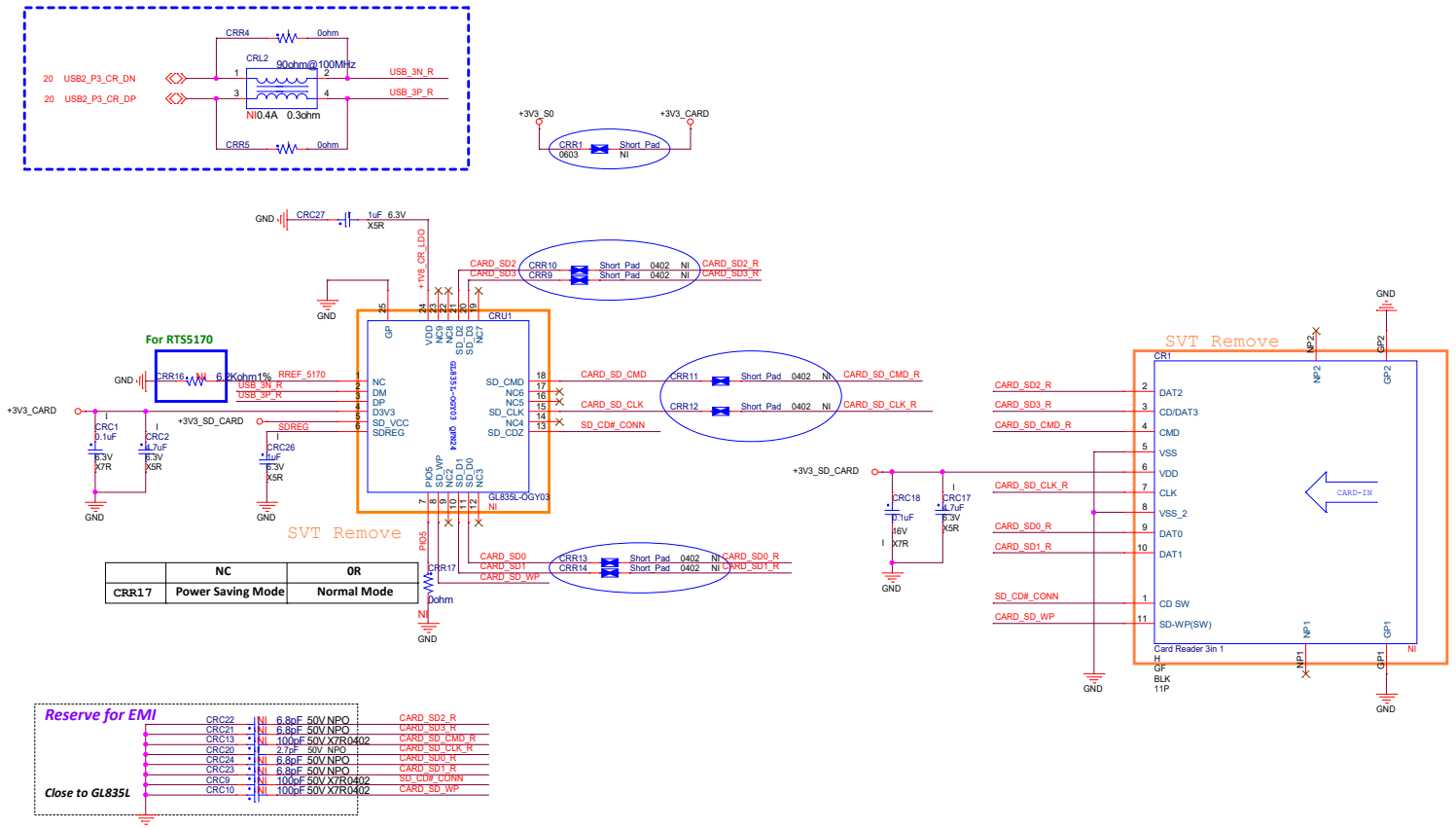
Asia Vital Components Co., Ltd.

CARD READER GL835L



	NC	0R
CRR17	Power Saving Mode	Normal Mode

Asia Vital Components Co., Ltd.		
Title: P31 SD Card USB2.0 GL835L		
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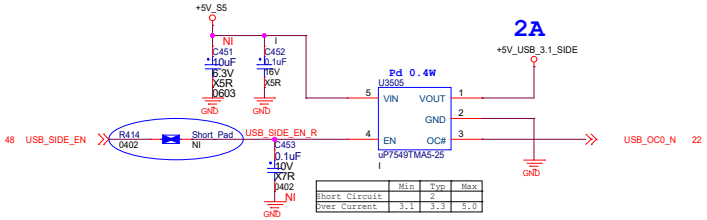
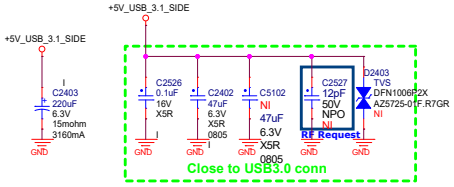
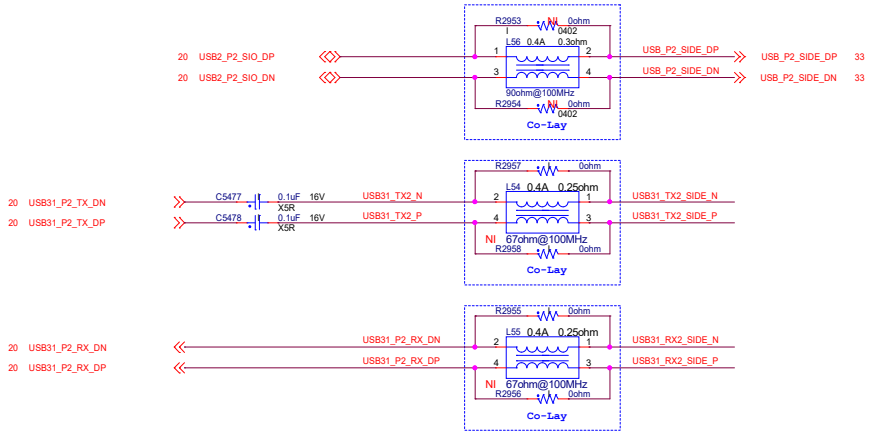
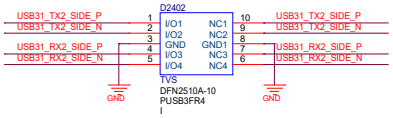
SIDE USB3.2 GEN2 Type-A (UP)

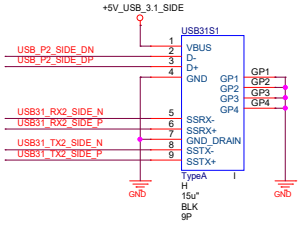




SIDE USB3.1 P1







AVC	Asia Vital Components Co., Ltd.		
Title	P32 USB3.1 SIDE1		
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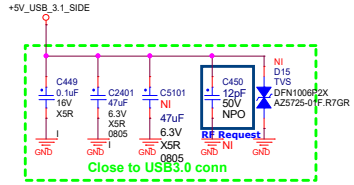
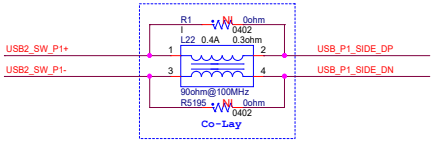
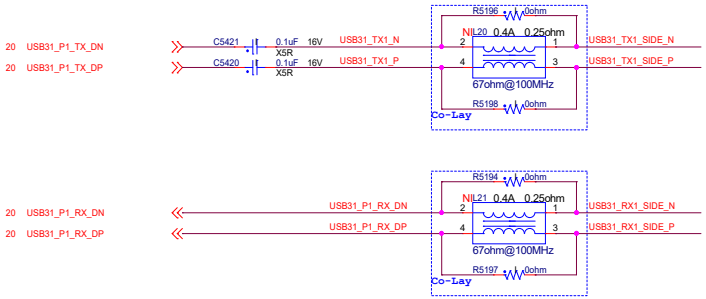
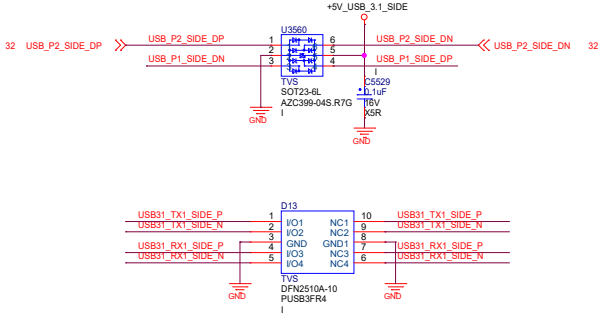
SIDE USB3.2 GEN2 Type-A (DOWN)

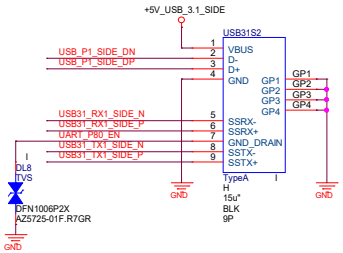




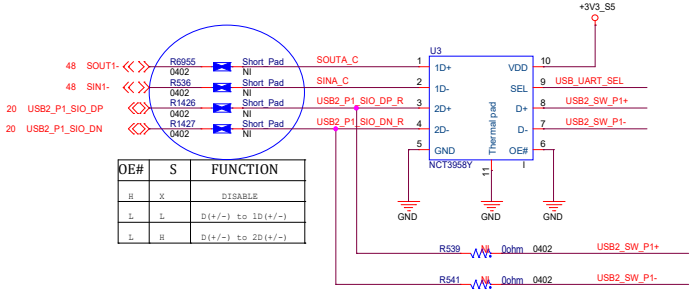




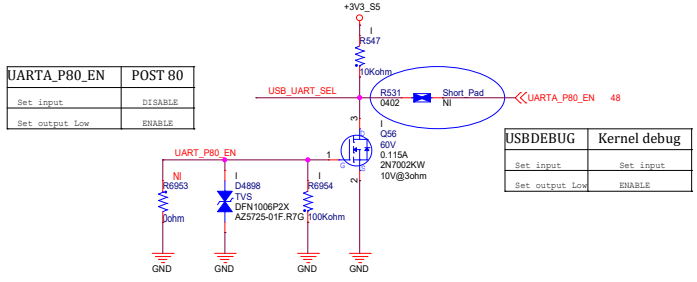
SIDE USB3.1 P2



USB Debug Function



OE#	S	FUNCTION
H	X	DISABLE
L	L	D(+/-) to 1D(+/-)
L	H	D(+/-) to 2D(+/-)



UARTA_P80_EN	POST 80
Set input	DISABLE
Set output Low	ENABLE

USBDEBUG	Kernel debug
Set input	Set input
Set output Low	ENABLE

Asia Vital Components Co., Ltd.	
Title: P33 USB3.1 SIDE2	
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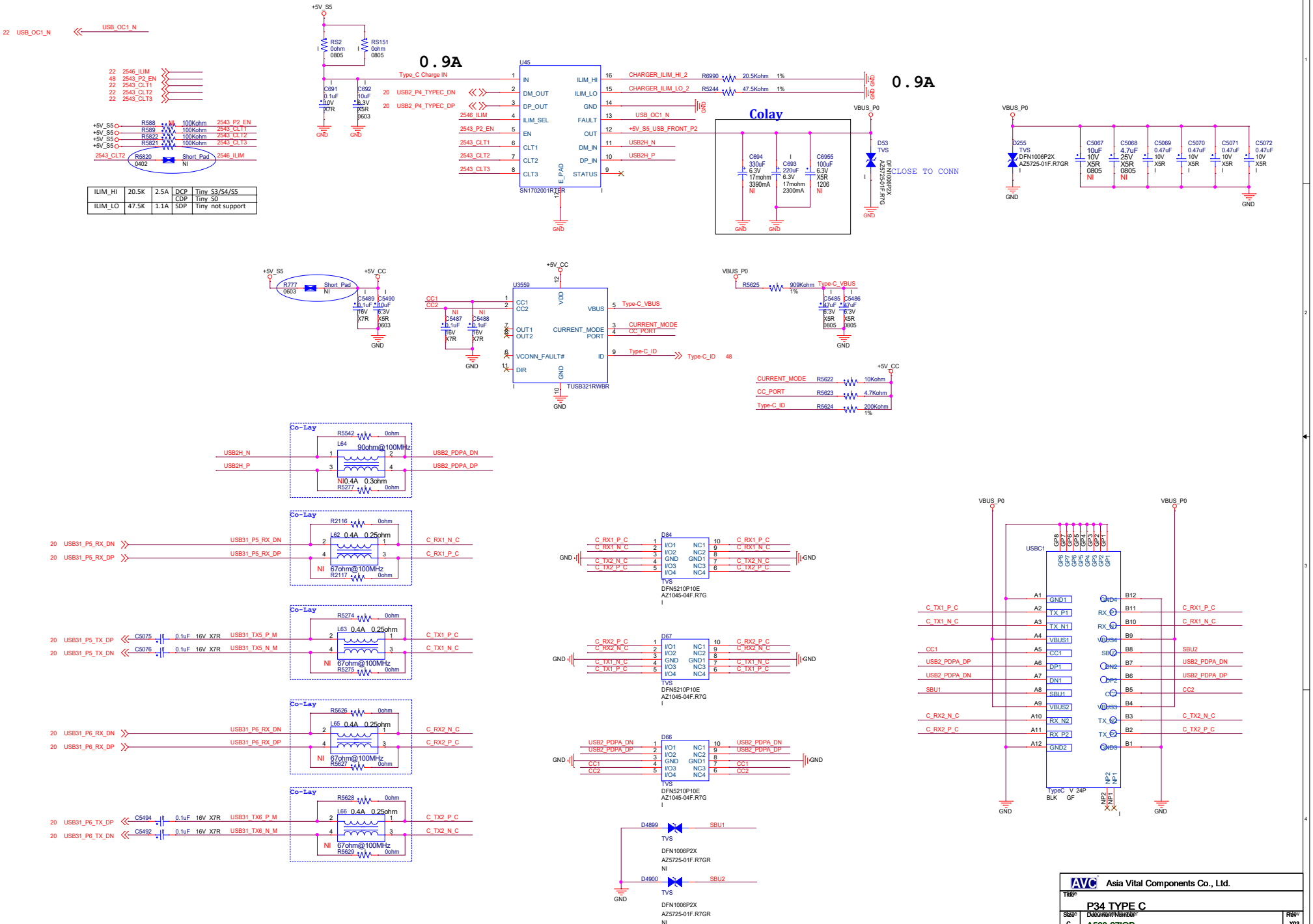
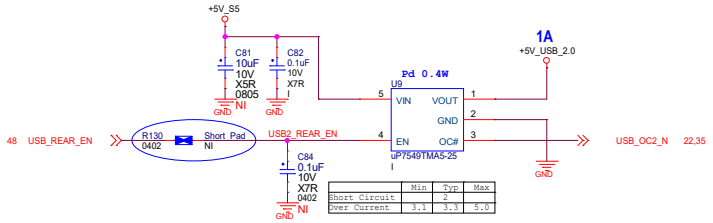
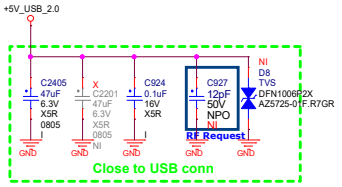
REAR IO - USB3.2 GEN1 Type-C

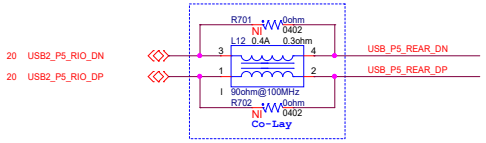


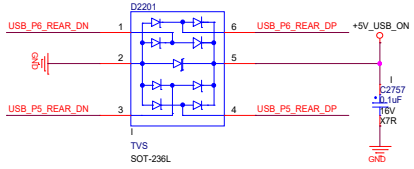
ILIM_HI	20.5K	2.5A	DCP	Tiny_S3/S4/S5
			CDP	Tiny_S0
ILIM_LO	47.5K	1.1A	SDP	Tiny_not support

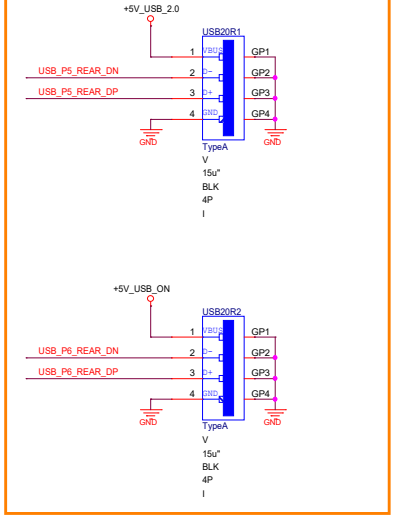
REAR USB2.0

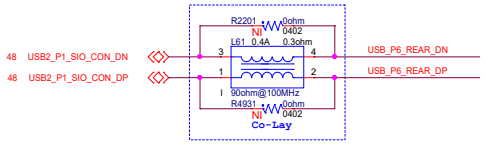












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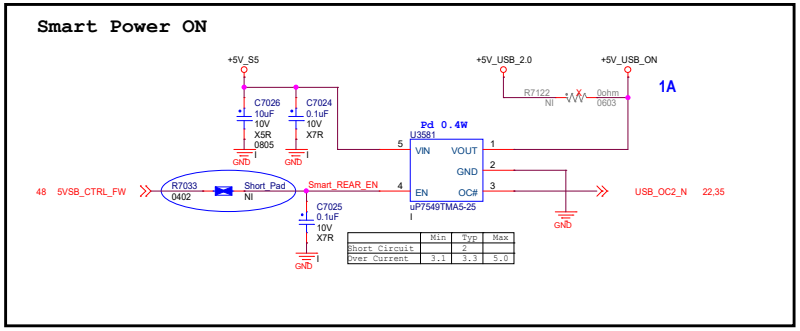

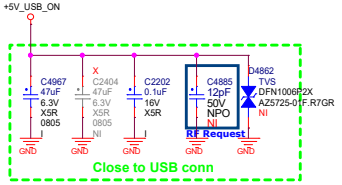

AVC Asia Vital Components Co., Ltd.			
Title: P35 USB2.0x2 REAR			
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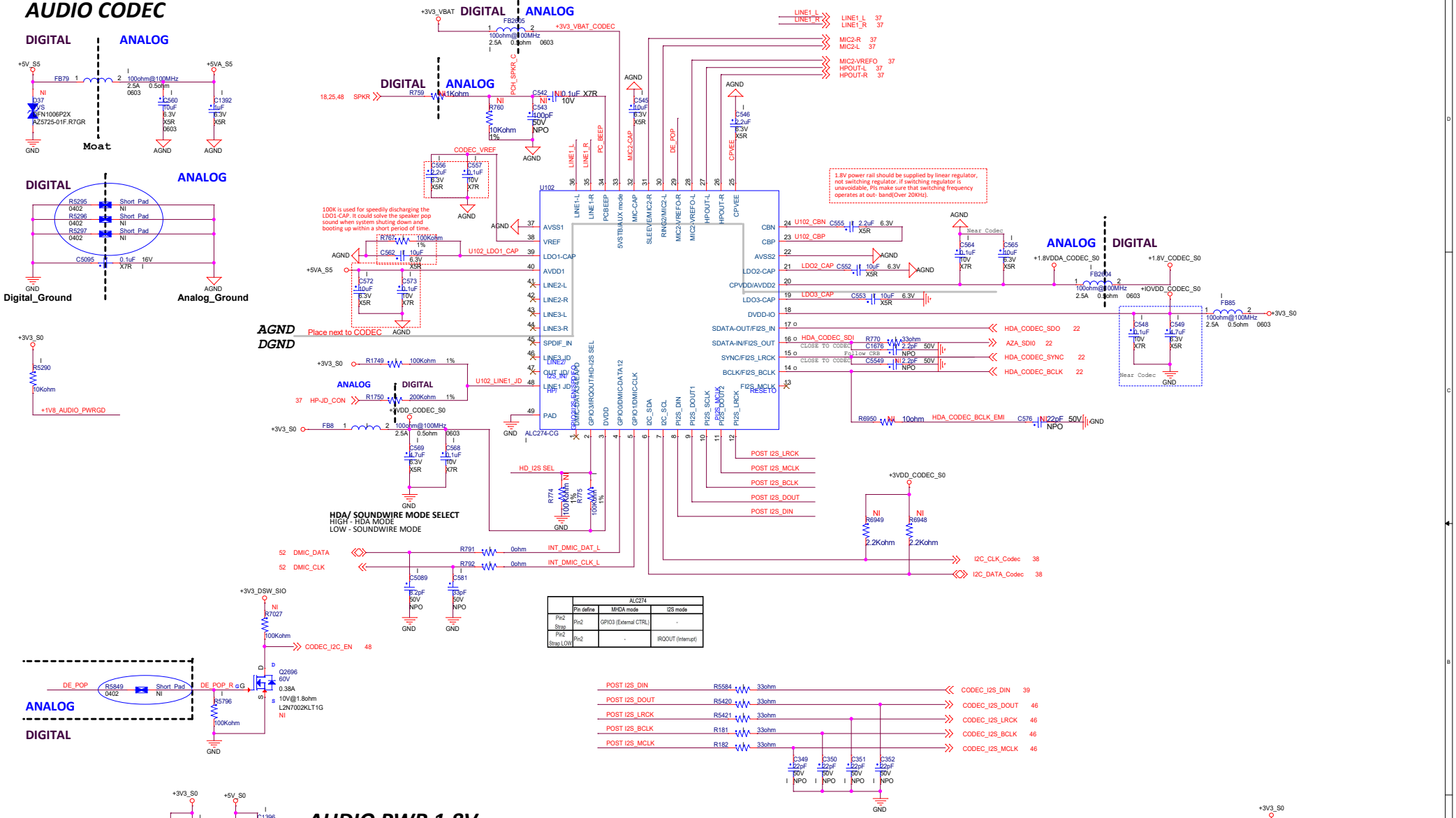
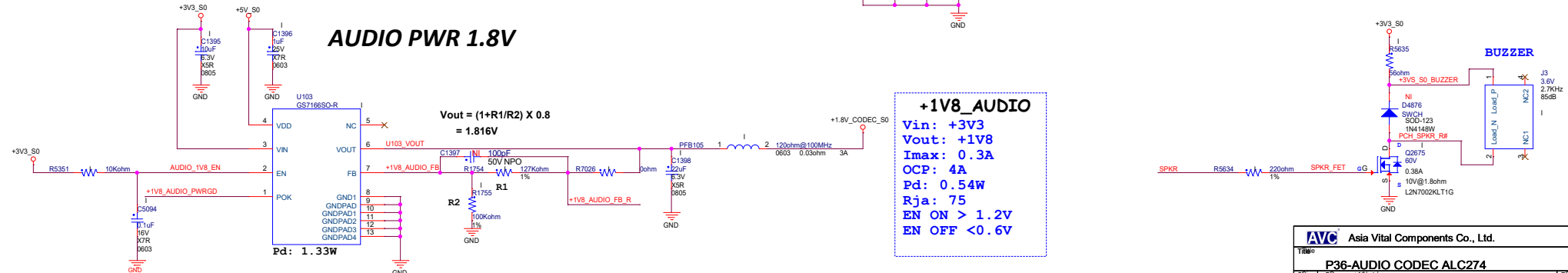
AUDIO CODEC



AUDIO PWR 1.8V



Asia Vital Components Co., Ltd.	
Title	P36-AUDIO CODEC ALC274
Size: C	Document Number: A560-27IOB
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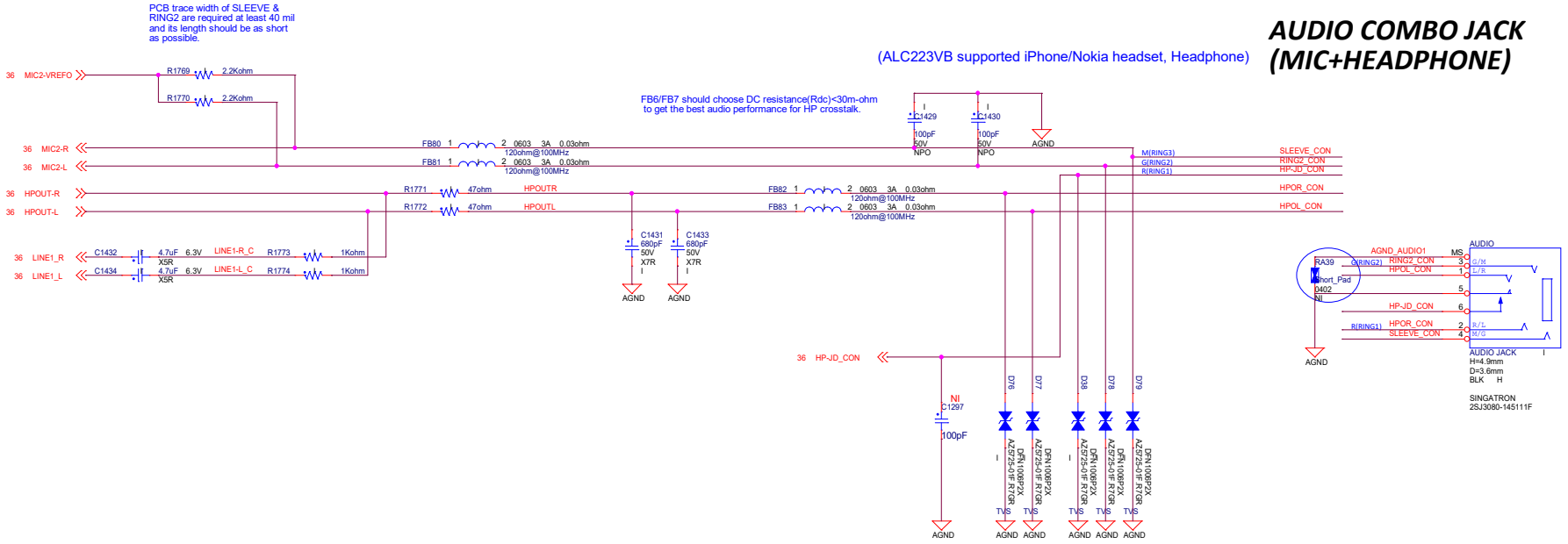
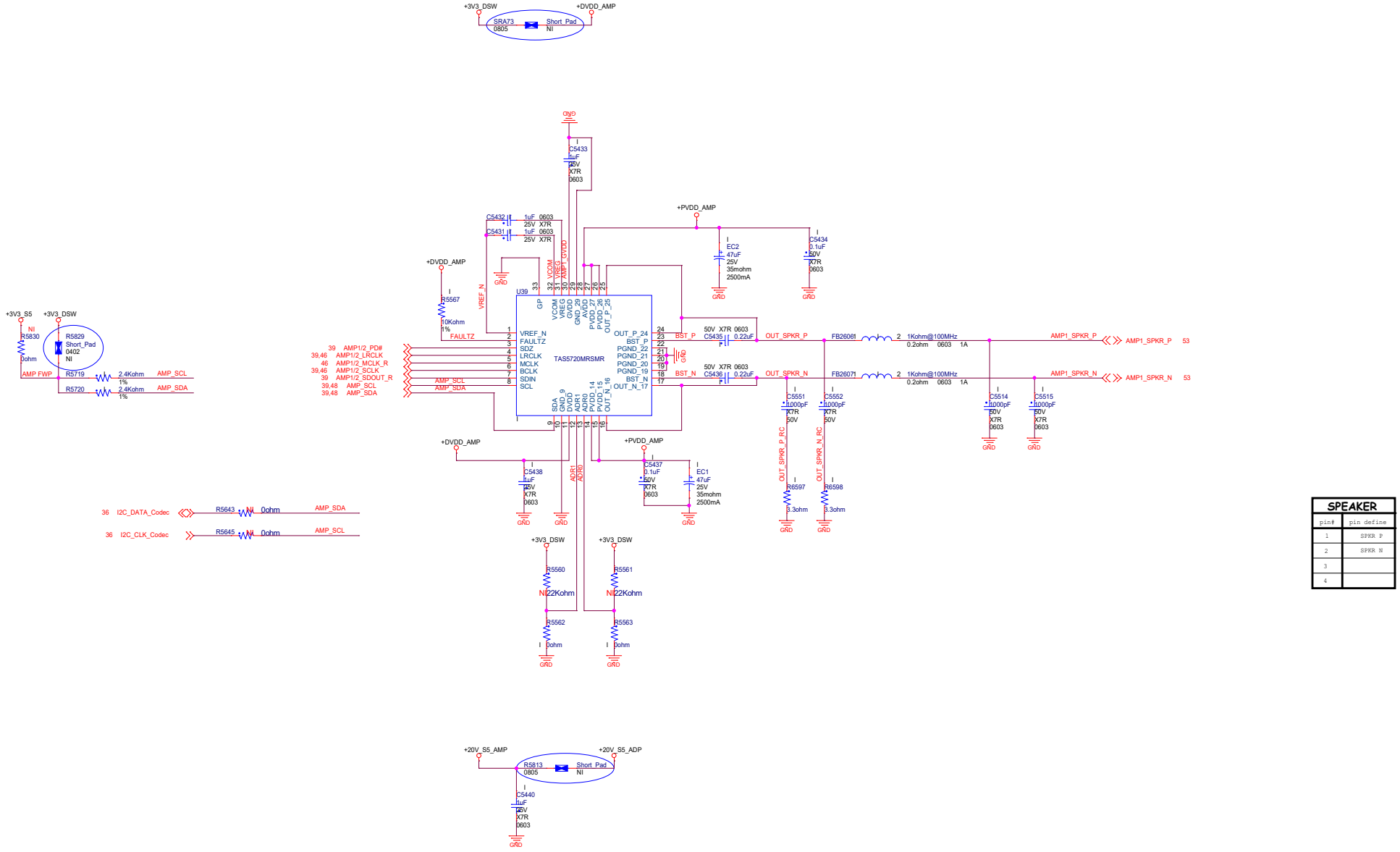
AUDIO COMBO JACK (MIC+HEADPHONE)

(ALC223VB supported iPhone/Nokia headset, Headphone)



Asia Vital Components Co., Ltd.			
Title: P37 Audio JACK			
Size: C	Document Number: A560-27IOB		Rev: X03
Date: Wednesday, February 24, 2021		Sheet 37 of 82	

Amp for first set SPKER



SPEAKER	
pin#	pin define
1	SPKR P
2	SPKR N
3	
4	

Asia Vital Components Co., Ltd.		
Title: P38 AUDIO 1ST AMP		
Size: C	Document Number: A560-27IOB	Rev: X03
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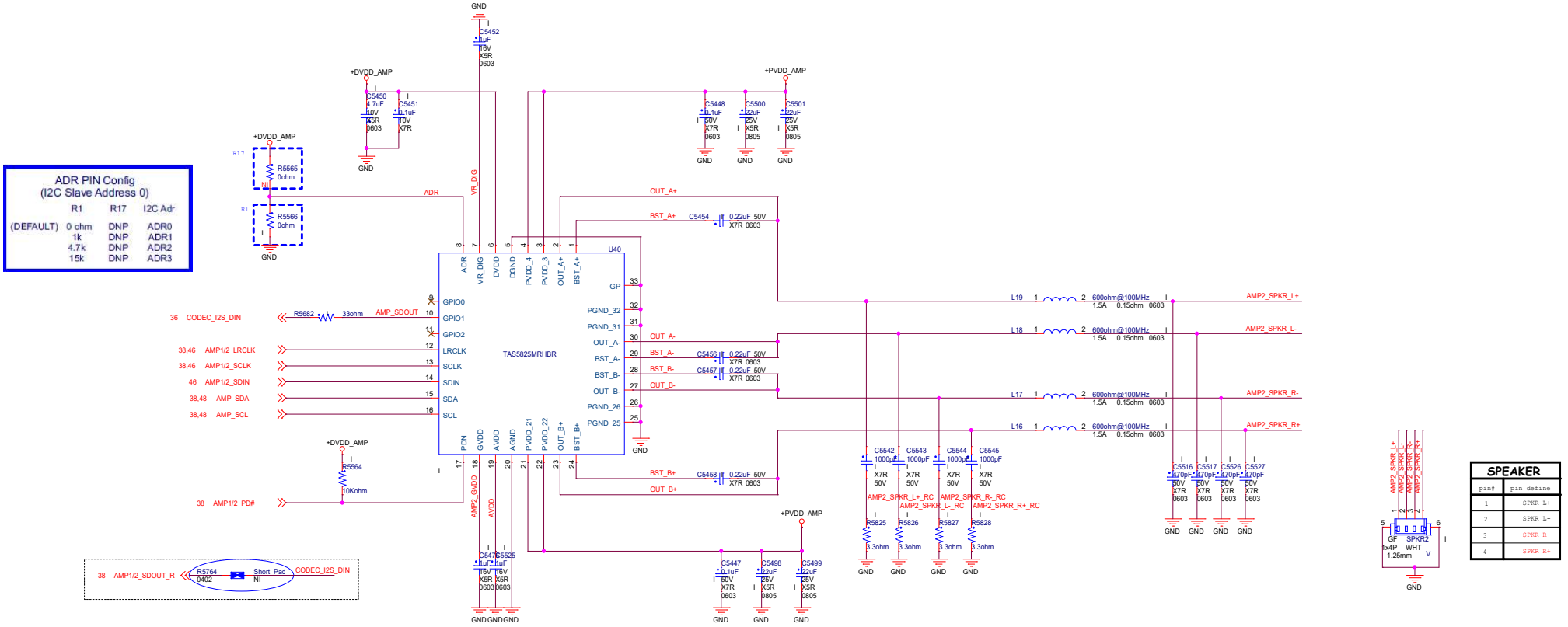
Amp for 2nd set SPKER



Asia Vital Components Co., Ltd.		
Title: P39 AUDIO 2ND AMP		
Size: C	Document Number: A560-27IOB	Rev: X03
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RESERVED

Asia Vital Components Co., Ltd.		
Title: P40 RESERVED		
Size: A	Document Number: A560-27IOB	Rev: X03
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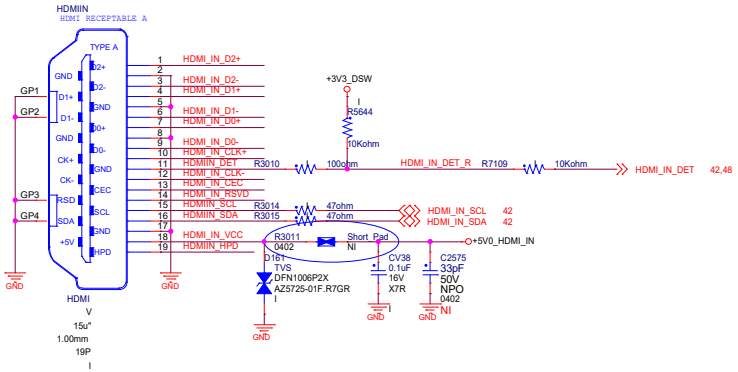
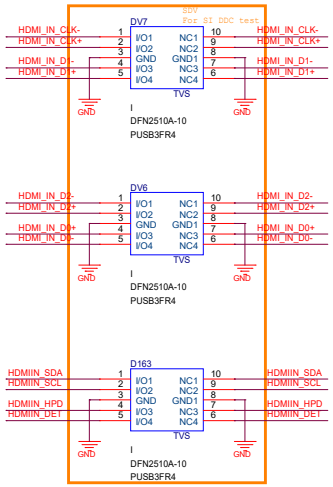
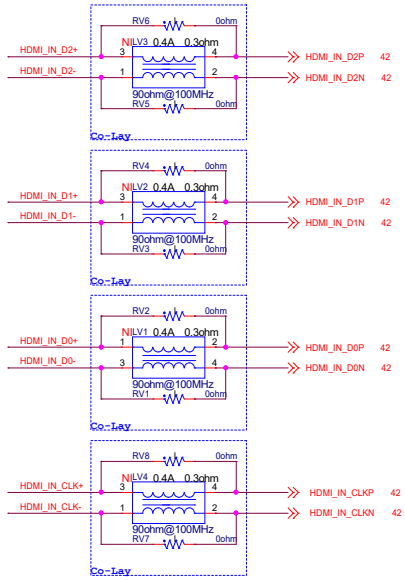
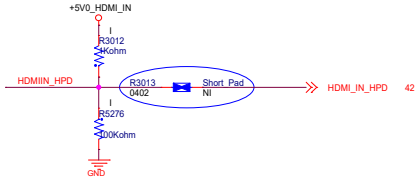
HDMI IN

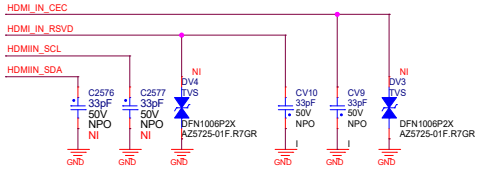


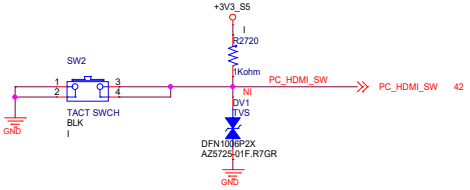
Layout swap pin



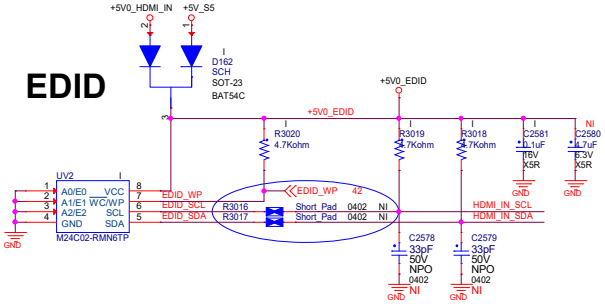








EDID



AVC Asia Vital Components Co., Ltd.			
Title: P41 HDMI IN			
Size: C	Document Number: A560-27IOB		Rev: X03
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Switch

46 DSP_I2S_SW#

+VLED_QHD

48,75 VBLCTRL
75 SCALAR_EDP_PWM_BKLCTL

41 HDMI_IN_SCL
41 HDMI_IN_SDA

R5683 Short_Pad 0402 NI
R5684 Short_Pad 0402 NI

LCDVDD (+10V)

74 S_ENVDD

48 EC_INT_BL

R5761 Short_Pad 0402 NI

SC_DDCINT

SCDDR_EN

44 DDR_PW_EN

VCCK_OFF_EN

44 VCCK_OFF_EN
41 EDID_WP
41,48 HDMI_IN_DET

+3V3_Scalar_RX

R5441 NI
R5442 6.2Kohm 1% / 12Kohm 1%

EDID_WP
TMDS_REXT

22 EDP_HPD

+3V3_Scalar_S5

HDMI_IN_DET
SC_WP_PRO
SC_EESCL
SC_EESDA
SC_HDMI_SCL
SC_HDMI_SDA

+1V1_Scalar_VCCK_ON
+DDR_SDRAM_SCA
+1V1_S5_Scalar_VCCK_OFF

ITLC 45
Panel_ID2 48,75
Panel_ID1 48,75
Panel_ID0 48,75

I2S_SD0_SC
I2S_MCK_SC
I2S_SCK_SC
I2S_WS_SC

C5283 NI / 2.2uF 6.3V X5R

DDR1_VREF

U3552

HDMI_CAB_DET1/GPIO/Test4b
TMDSREXT
eCBUS3/GPIO/HDMI_HPD
RX_33V
RX0P_3
RX0N_3
RX2P_3/MHLP
RX2N_3/MHLN
TMDS_GND_1
RX1P_3
RX1N_3
RX0P_3
RX0N_3
GDI_11V
eCBUS2/GPIO/HDMI_HPD
RX_33V
RX0P_2
RX0N_2
RX2P_2/MHLP
RX2N_2/MHLN
TMDS_GND_3
RX1P_2
RX1N_2
RX0P_2
RX0N_2
GDI_11V
eCBUS1/GPIO
RX_33V
LANE0P_1
LANE0N_1
DP_GND_1
LANE1P_1
LANE1N_1
DP_GND_2
LANE2P_1
LANE2N_1
DP_GND_3
LANE3P_1
LANE3N_1
GDI_11V
LANE0P_0
LANE0N_0
DP_GND_4
LANE1P_0
LANE1N_0
DP_GND_5
LANE2P_0
LANE2N_0
DP_GND_6
LANE3P_0
LANE3N_0
GDI_11V
DP_CAB_DET0_0/TCON[0]/GPIO/Test4b
DP_CAB_DET1_0/TCON[8]/GPIO/Test4b

HDMI_CAB_DET2/GPIOTest4b
DDCSDA3/GPIO
DDCSCL3/GPIO
DDCSDA2/GPIO
DDCSCL2/GPIO
EE2CSDA/PWM1/TCON[2]/GPIO
EE2CSCL/PWM0/TCON[3]/GPIO
EEWDFN/SDO/GPIOTest4b
CEC/GPIOTest4b
PGND_2
PVCC
DP_CAB_DET1_1/TCON[9]/GPIO/Test4b
DP_CAB_DET0_1/TCON[0]/GPIO/Test4b
DP_CAB_DET0_1/TCON[12]/GPIO/Test4b
DP_CAB_DET0_2/TCON[13]/GPIO/Test4b
DP_HPD_0/UART_TX/GPIOTest4b
DP_HPD_1/Int0/UART_RX/GPIOTest4b
Edid WP/PWM3/IICSDA_2/TCON[9]/GPIO
PCB_POWE_DOWN/ICSCL_2/PWM4/TCON[11]/GPIO
LED_PWM/IICSCL_2/PWM5/TCON[10]/GPIO
DP_HPD_2/UART_TX/GPIOTest4b
DP_HPD_3/UART_RX/GPIOTest4b
MHL_HDMI_SW/TCON[4]/GPIO/Test4b
MHL_HDMI_1.5W/TCON[5]/GPIO/Test4b
MHL_POWER_SW/TCON[6]/GPIO/Test4b
MHL_POW_SW1/PWM2_1/TCON[1]/IR_RECEIVER/GPIO
VCCK_ON
RESETB
SCA_SPI_WP#
SCA_SPI_HOLD#
SCA_SPI_CS#
SCA_SPI_SDI
SCA_SPI_SDO
SCA_SPI_CK
SPI_CEB
SPI_SO
SPI_CK
SPI_SI
DDR1_V25SDRAM_V33
GPIO/TCON[6]/IICSCL_1
DDR1_VREF
GPIO/TCON[7]/IICSDA_1
GPIO/TCON[6]/IICSCL_1
LED1/PWM1/TCON[14]/GPIOTest4b
DDR1_V25SDRAM_V33
PGND_1
PWM1_0/DPTX_AUX_CH_N_1/TCON[7]/GPIO
PWM3/DPTX_AUX_CH_P_1/TCON[15]/GPIO
DPTX_HPD_1/TCON[8]/GPIO
USB_SPI_CEB0/IR2B/GPIOBacklight_adjustment/DVS
USB_SPI_CEB1/IR2F/GPIO/BacklightOnOff
USB_SPI_SI/GPIO/AudioDACmute/TI
USB_SPI_CLK/CLKO/GPIO/AudioDACadjust/TO
SPDIF/I2SDO/GPIOTest4b
SCK/TCON[13]/GPIOTest4b
WS/TCON[12]/GPIOTest4b
PVCC
PAD

RTD2785T-CG

I2S

I2S_SCK_SC R5479 0ohm I2S_BCLK_SW_SC 46
I2S_WS_SC R5480 0ohm I2S_LRCK_SW_SC 46
I2S_SD0_SC R5481 0ohm I2S_DOUT_SW_SC 46
I2S_MCK_SC R5648 0ohm I2S_MCK_SW_SC 46

C5519 NI 10pF 50V NPO I2S_BCLK_SW_SC
C5520 NI 10pF 50V NPO I2S_LRCK_SW_SC
C5521 NI 10pF 50V NPO I2S_DOUT_SW_SC
C5522 NI 10pF 50V NPO I2S_MCK_SW_SC

GND

+3V3_Scalar_S5

R5473 4.7Kohm
RESETB
C5307 10uF 6.3V X5R 0603

GND

VCCK_OFF
TXA0N_10b/TXA0N_8b/GPIO
TXA0P_10b/TXA0P_8b/GPIO
TXA1N_10b/TXA1N_8b/GPIO
TXA1P_10b/TXA1P_8b/GPIO
TXA2N_10b/TXA2N_8b/GPIO
TXA2P_10b/TXA2P_8b/GPIO
TXACN_10b/TXACN_8b/GPIO
TXACP_10b/TXACP_8b/GPIO
TXA3N_10b/TXA3N_8b/GPIO
TXA3P_10b/TXA3P_8b/GPIO
TXA4N_10b/GPIO
TXA4P_10b/GPIO
PVCC
TXB0N_10b/TXB0N_8b/GPIO
TXB0P_10b/TXB0P_8b/GPIO
TXB1N_10b/TXB1N_8b/GPIO
TXB1P_10b/TXB1P_8b/GPIO
TXB2N_10b/TXB2N_8b/GPIO
TXB2P_10b/TXB2P_8b/GPIO
TXB3N_10b/TXB3N_8b/GPIO
TXB3P_10b/TXB3P_8b/GPIO
TXB4N_10b/GPIO
TXB4P_10b/GPIO
VCCK_OFF
TXC0N_10b/TXC0N_8b
TXC0P_10b/TXC0P_8b
TXC1N_10b/TXC1N_8b
TXC1P_10b/TXC1P_8b
TXC2N_10b/TXC2N_8b
TXC2P_10b/TXC2P_8b
TXCCN_10b/TXCCN_8b
TXCCP_10b/TXCCP_8b
TXC3N_10b/TXC3N_8b/DPTX_LANE_P<0>
TXC3P_10b/TXC3P_8b/DPTX_LANE_N<0>
DPTX_VDD11
TXC4N_10b/DPTX_LANE_P<1>
TXC4P_10b/DPTX_LANE_N<1>
DPTX_VDD33
TXD0N_10b/TXD0N_8b/DPTX_LANE_P<2>
TXD0P_10b/TXD0P_8b/DPTX_LANE_N<2>
DPTX_VDD11
TXD1N_10b/TXD1N_8b/DPTX_LANE_P<3>
TXD1P_10b/TXD1P_8b/DPTX_LANE_N<3>
TXD2N_10b/TXD2N_8b
TXD2P_10b/TXD2P_8b
TXD3N_10b/TXD3N_8b
TXD3P_10b/TXD3P_8b
NC_9
TXD4N_10b
TXD4P_10b
VCCK_OFF
DDR1_V25/SDRAM_V33
AUDIO_VDD33

+1V1_S5_Scalar_VCCK_OFF
+3V3_Scalar_S5
+1V1_S5_Scalar_VCCK_OFF
+DDR_SDRAM_SCA
+3V3_Scalar_AUDIO

LVDS_TXA0N 45
LVDS_TXA0P 45
LVDS_TXA1N 45
LVDS_TXA1P 45
LVDS_TXA2N 45
LVDS_TXA2P 45
LVDS_TXACN 45
LVDS_TXACP 45
LVDS_TXA3N 45
LVDS_TXA3P 45
LVDS_TXB0N 45
LVDS_TXB0P 45
LVDS_TXB1N 45
LVDS_TXB1P 45
LVDS_TXB2N 45
LVDS_TXB2P 45
LVDS_TXB3N 45
LVDS_TXB3P 45
LVDS_TXC0N 45
LVDS_TXC0P 45
LVDS_TXC1N 45
LVDS_TXC1P 45
LVDS_TXC2N 45
LVDS_TXC2P 45
LVDS_TXCCN 45
LVDS_TXCCP 45
LVDS_TXC3N 45
LVDS_TXC3P 45
LVDS_TXD0N 45
LVDS_TXD0P 45
LVDS_TXD1N 45
LVDS_TXD1P 45
LVDS_TXD2N 45
LVDS_TXD2P 45
LVDS_TXD3N 45
LVDS_TXD3P 45

10 EDP_TXP0 / 10 EDP_TXN0 — C5268 / C5269 0.1uF 10V X7R — EDP_TXP0_C / EDP_TXN0_C
10 EDP_TXP1 / 10 EDP_TXN1 — C5270 / C5271 0.1uF 10V X7R — EDP_TXP1_C / EDP_TXN1_C
10 EDP_TXP2 / 10 EDP_TXN2 — C5272 / C5273 0.1uF 10V X7R — EDP_TXP2_C / EDP_TXN2_C
10 EDP_TXP3 / 10 EDP_TXN3 — C5274 / C5275 0.1uF 10V X7R — EDP_TXP3_C / EDP_TXN3_C

41 PC_HDMI_SW

BOTTON ON/OFF CHANGE

41 HDMI_IN_HPD
41 HDMI_IN_CLKN
41 HDMI_IN_CLKP
41 HDMI_IN_D0N
41 HDMI_IN_D0P
41 HDMI_IN_D1N
41 HDMI_IN_D1P
41 HDMI_IN_D2N
41 HDMI_IN_D2P

+1V1_S5_Scalar_GDI
+3V3_Scalar_RX2

+3V3_Scalar_S5

R5456 4.7Kohm SCA_SPI_CS#
R5457 4.7Kohm SCA_SPI_WP#
R5460 10Kohm SCA_SPI_HOLD#
R5464 4.7Kohm SC_EESCL
R5465 4.7Kohm SC_EESDA
R5466 4.7Kohm SC_WP_PRO_R
R5467 2.2Kohm SC_DDCSCL
R5468 2.2Kohm SC_DDCSDA
R5474 4.7Kohm S_ENVDD
R5476 10Kohm EDID_WP
R5762 4.7Kohm EC_INT_BL

R5721 10Kohm ITLC

R5475 100Kohm VBLCTRL
R5458 4.7Kohm SCA_SPI_CS#
R5459 4.7Kohm SCA_SPI_WP#

GND

PCH

+3V3_Scalar_ADC
+3V3_Scalar_S5
+1V1_Scalar_VCCK_ON

NI TP4870
NI TP4871
1TSC1
1TSC2

10 EDP_AUXP — C5277 0.1uF 10V X7R — EDP_AUXP_SC
10 EDP_AUXN — C5276 0.1uF 10V X7R — EDP_AUXN_SC

R5443 Short_Pad 0402 NI
R5444 Short_Pad 0402 NI

45 SCALAR_CLK
45 SCALAR_DATA

EDP_AUXP_SC
EDP_AUXN_SC
SC_SMLDAT

ADC_VDD33
AHS
B-
B+
G-
G+
R-
R+
SOG
ADC_GND
DDCSCL_VGA/GPIO
DDCSDA_VGA/GPIO
VGA_CAB_DET_0/PWM0/TCON[4]/GPIO/Test4b
PVCC
VCCK_ON
DDCSCL_AUXP_D0/GPIO
DDCSDA_AUXN_D0/GPIO
DDCSCL1/DDCSCL_AUXP_D1/GPIO
DDCSDA1/DDCSDA_AUXN_D1/GPIO
NC_2
DPTX_VDD11
NC_3
NC_4
DPTX_VDD33
NC_5
NC_6
DPTX_VDD11
NC_7
NC_8
XI
XO
DDR1_V25/SDRAM_V33
DPTX_AUX_CH_P/GPIO
DPTX_AUX_CH_N/GPIO
A-ADC2/INT1/GPIOTest4b
A-ADC1/INT1/GPIOTest4b
MHL_CABLE_DET/0TCON[9]/A-ADC2/GPIO/Test4b
MHL_CABLE_DET1/TCON[10]/A-ADC3/GPIO/Test4b
PVCC
VCCK_ON
GPIO/pwm_out/PWM1
AUDIO_HPVDD
AUDIO_HOUTL/SD2/SPDIF2/GPIO
AUDIO_HOUTR/SD3/SPDIF3/GPIO
AUDIO_HP_GND
AUDIO_HP_AVDD
LINE_IN/VG/GPIO
LINE_IN/RSCK/GPIO
AUDIO_REF/MCK/GPIO
AUDIO_SOUTL/SD1/SPDIF1/GPIO
AUDIO_SOUTR/SD1/SPDIF1/GPIO
AUDIO_GND

RTD2785T-CG

AUDIO_GND
AUDIO_REF C5278 1uF 6.3V X5R AUDIO_GND
+3V3_Scalar_AUDIO_HP
SCALAR_EDP_PWM_BKLCTL
PCH_EDP_BKLTCTL 22
+1V1_Scalar_VCCK_ON
+3V3_Scalar_S5

R5446 Short_Pad 0402 NI SCA_XO
R5447 Short_Pad 0402 NI SCA_XI

Y8 14.318180MHZ 12pF +/-20PPM
R5445 1Mohm 1%
C5285 12pF 50V NPO
C5284 12pF 50V NPO

SCA_SPI_CS# R5453 22ohm SCA_SPI_CS#_R
SCA_SPI_SDO R5454 22ohm SCA_SPI_SDO_R
SCA_SPI_WP# R5455 22ohm SCA_SPI_WP#_R

U3555
/CS VCC
DO (IO1) /HOLD (IO3)
/WP (IO2) CLK
GND DI (IO0)
W25Q16JVSSIM

C5299 0.1uF 16V X5R
C5300 NI 0.1uF 16V X5R 0402

SCA_SPI_HOLD# R5452 22ohm SCA_SPI_HOLD
SCA_SPI_CK_R R5451 22ohm SCA_SPI_CK
SCA_SPI_SDI_R R5452 22ohm SCA_SPI_SDI

U3556
NC1 VCC
NC2 WC
NC3 SCL
GND SDA
M24C16-WMN6TP

C5301 0.1uF 16V X5R

SC_WP_PRO_R R5463 47ohm SC_WP_PRO
SC_EESCL_R R5461 Short_Pad 0402 NI SC_EESCL
SC_EESDA_R R5462 Short_Pad 0402 NI SC_EESDA

EC

SC_DDCSCL — Q2663A 50V 0.2A 5V@3.5ohm LBSS138DW1T1G — EC_SMLCLK_BL 48
SC_DDCSDA — Q2663B 50V 0.2A 5V@3.5ohm LBSS138DW1T1G — EC_SMLDAT_BL 48

Asia Vital Components Co., Ltd.			
Title: P42 RTD2785T-CG			
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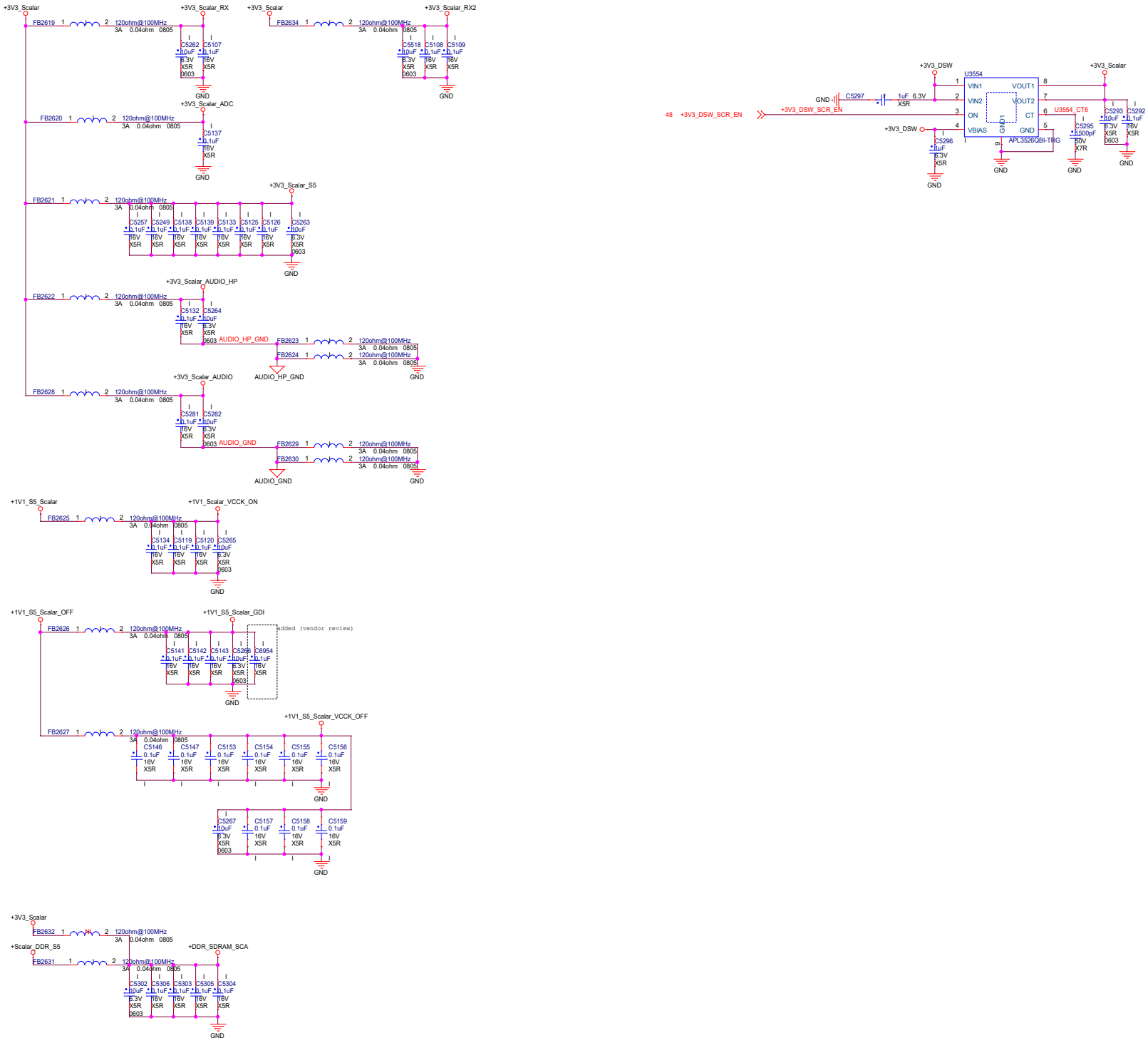

Asia Vital Components Co., Ltd.		
Title: P43 Scalar POWER		
Size: C	Document Number: A560-27IOB	Rev: X03
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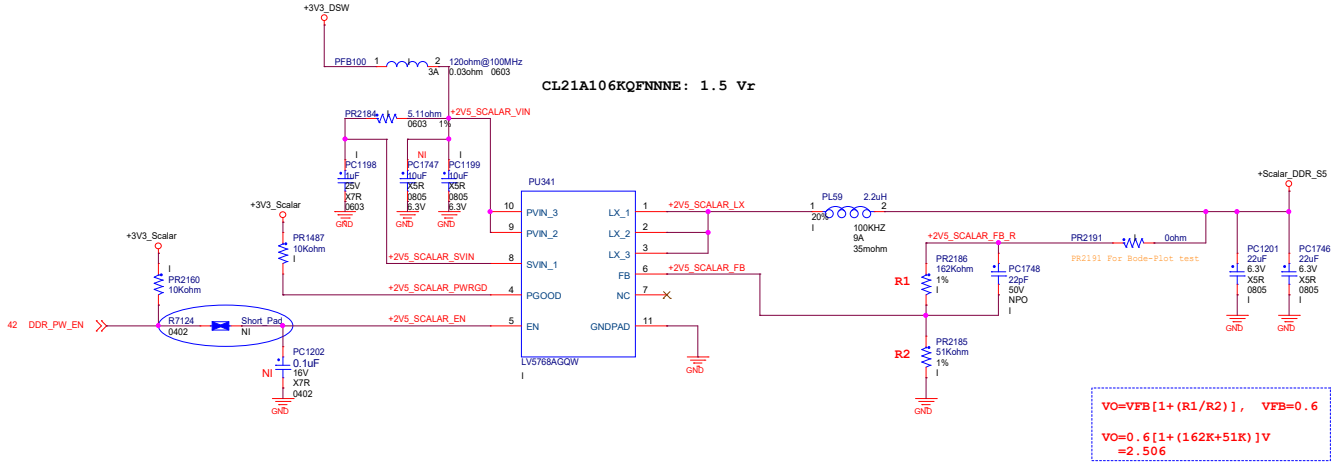
+Scalar_DDR_S5

Max Load:0.5A CONVERTER

Vout	2.5V
Vin	3.3V
Switch Freq	1MHz
ocp	4A
Vin_Iripple	10uF/1A
Choke size	2.2uH / 5.5x5.0mm
Choke Idc/Isat	5.5A / 9.0A
Choke DCR	35mohm
Cin CAP	10uF
Cout CAP	22uF x2
Cout CAP_ESR LIR	



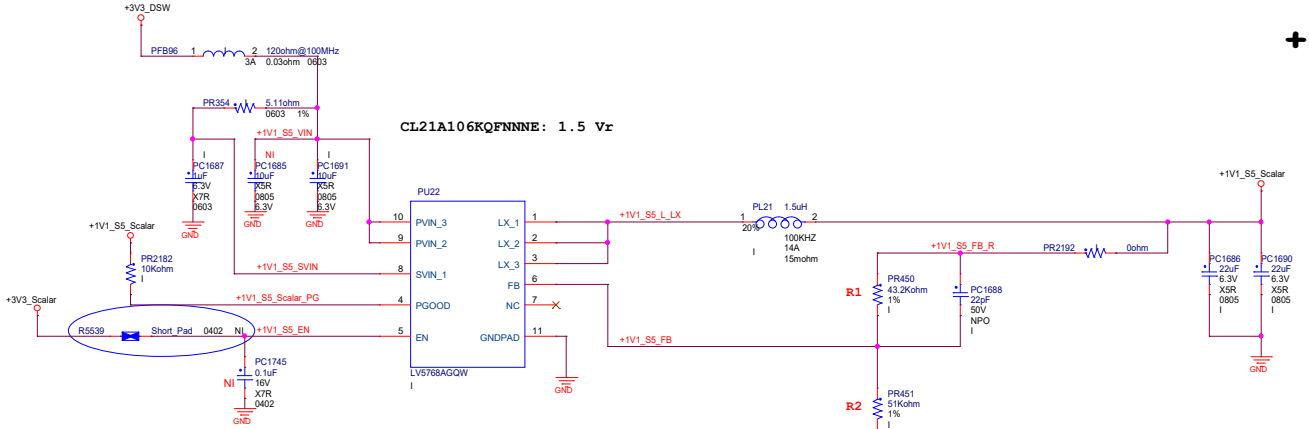
VO=VFB[1+(R1/R2)], VFB=0.6

VO=0.6[1+(162K+51K)]V
=2.506

+1V1_S5_Scalar

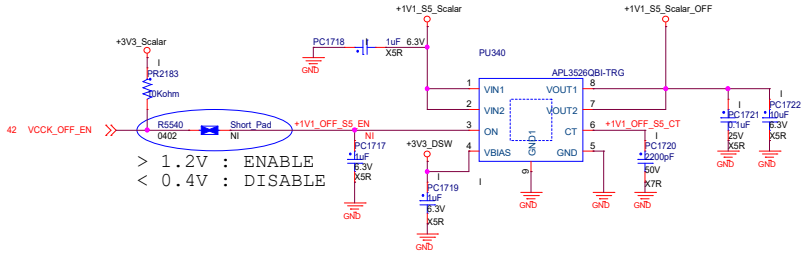
Max Load:0.5A CONVERTER

Vout	1.1V
Vin	3.3V
Switch Freq	1MHz
ocp	4A
Vin_Iripple	10uF/1A
Choke size	1.5uH / 7.6x6.8mm
Choke Idc/Isat	9A / 14A
Choke DCR	15mohm
Cin CAP	10uF
Cout CAP	22uFx2
Cout CAP_ESR LIR	



VO=VFB(1+(R1/R2)), VFB=0.6

VO=0.6[1+(43.2K/51K)]
=1.108V



Asia Vital Components Co., Ltd.			
Title: P44 +1V1_S5_Scalar_QHD			
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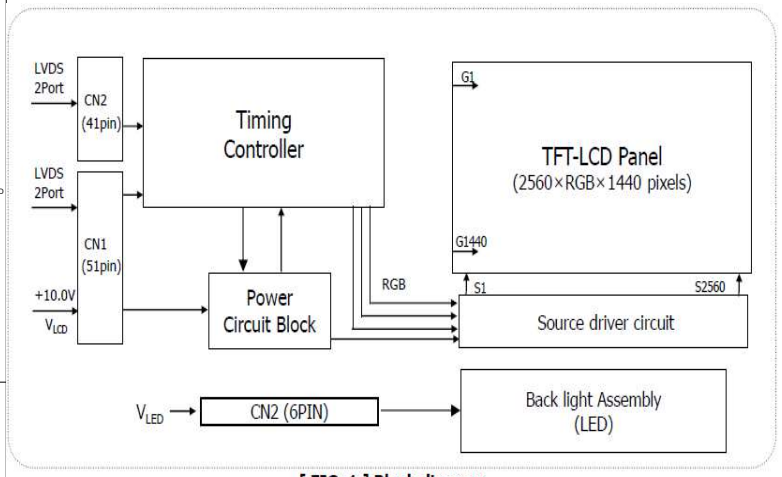


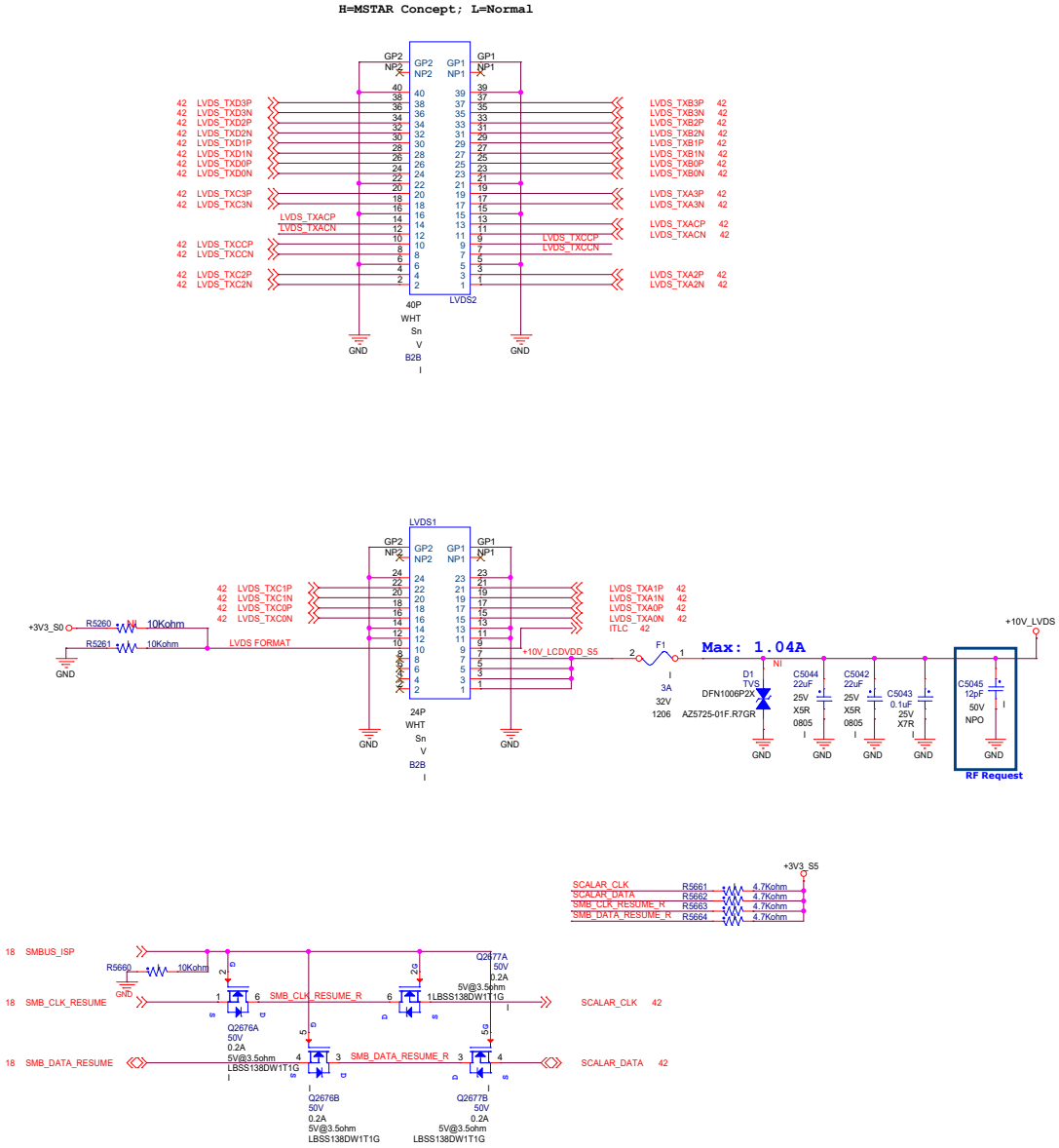
[FIG. 1] Block diagram

Table 3-1. MODULE CONNECTOR(CN1) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	GND	Ground	27	NC	No Connection
2	NC	No Connection	28	R2AN	SECOND LVDS Receiver Signal (A-)
3	NC	No Connection	29	R2AP	SECOND LVDS Receiver Signal (A+)
4	NC	No Connection	30	R2BN	SECOND LVDS Receiver Signal (B-)
5	NC	No Connection	31	R2BP	SECOND LVDS Receiver Signal (B+)
6	ITLC	Ground	32	R2CN	SECOND LVDS Receiver Signal (C-)
7	LVDS Format	'H'(3.3V)= MSTAR Concept, 'L'=normal (Connect High or low, No NC Condition)	33	R2CP	SECOND LVDS Receiver Signal (C+)
8	NC	No Connection	34	GND	Ground
9	NC	No Connection	35	R2CLKN	SECOND LVDS Receiver Clock Signal(-)
10	PWM_OUT	Reference signal for LED Driver control	36	R2CLKP	SECOND LVDS Receiver Clock Signal(+)
11	GND	Ground	37	GND	Ground
12	R1AN	FIRST LVDS Receiver Signal (A-)	38	R2DN	SECOND LVDS Receiver Signal (D-)
13	R1AP	FIRST LVDS Receiver Signal (A+)	39	R2DP	SECOND LVDS Receiver Signal (D+)
14	R1BN	FIRST LVDS Receiver Signal (B-)	40	NC	No Connection
15	R1BP	FIRST LVDS Receiver Signal (B+)	41	NC	No Connection
16	R1CN	FIRST LVDS Receiver Signal (C-)	42	Reserved	No connection or GND
17	R1CP	FIRST LVDS Receiver Signal (C+)	43	Reserved	No connection or GND
18	GND	Ground	44	GND	Ground
19	R1CLKN	FIRST LVDS Receiver Clock Signal(-)	45	GND	Ground
20	R1CLKP	FIRST LVDS Receiver Clock Signal(+)	46	GND	Ground
21	GND	Ground	47	NC	No connection
22	R1DN	FIRST LVDS Receiver Signal (D-)	48	VLCD	Power Supply +10.0V
23	R1DP	FIRST LVDS Receiver Signal (D+)	49	VLCD	Power Supply +10.0V
24	NC	No Connection	50	VLCD	Power Supply +10.0V
25	NC	No Connection	51	VLCD	Power Supply +10.0V
26	Reserved	No connection or GND	-	-	-

Table 3-2. MODULE CONNECTOR(CN2) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	NC	No connection(Reserved)	22	NC	No Connection
2	NC	No connection	23	NC	No Connection
3	NC	No connection	24	GND	Ground
4	NC	No connection	25	GND	Ground
5	NC	No connection	26	R4AN	FORTH LVDS Receiver Signal (A-)
6	NC	No connection	27	R4AP	FORTH LVDS Receiver Signal (A+)
7	NC	No connection	28	R4BN	FORTH LVDS Receiver Signal (B-)
8	NC	No connection	29	R4BP	FORTH LVDS Receiver Signal (B+)
9	GND	Ground	30	R4CN	FORTH LVDS Receiver Signal (C-)
10	R3AN	THIRD LVDS Receiver Signal (A-)	31	R4CP	FORTH LVDS Receiver Signal (C+)
11	R3AP	THIRD LVDS Receiver Signal (A+)	32	GND	Ground
12	R3BN	THIRD LVDS Receiver Signal (B-)	33	R4CLKN	FORTH LVDS Receiver Clock Signal(-)
13	R3BP	THIRD LVDS Receiver Signal (B+)	34	R4CLKP	FORTH LVDS Receiver Clock Signal(+)
14	R3CN	THIRD LVDS Receiver Signal (C-)	35	GND	Ground
15	R3CP	THIRD LVDS Receiver Signal (C+)	36	R4DN	FORTH LVDS Receiver Signal (D-)
16	GND	Ground	37	R4DP	FORTH LVDS Receiver Signal (D+)
17	R3CLKN	THIRD LVDS Receiver Clock Signal(-)	38	NC	No Connection
18	R3CLKP	THIRD LVDS Receiver Clock Signal(+)	39	NC	No Connection
19	GND	Ground	40	GND	Ground
20	R3DN	THIRD LVDS Receiver Signal (D-)	41	GND	Ground
21	R3DP	THIRD LVDS Receiver Signal (D+)	-		



AVC	Asia Vital Components Co., Ltd.		
Title	P45-LVDS CONNECTOR_QHD		
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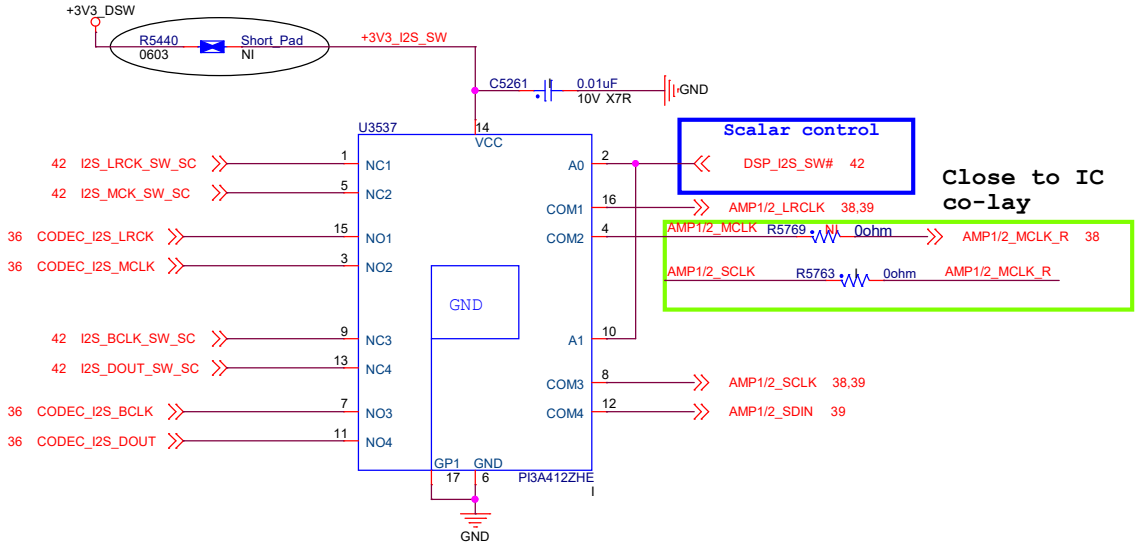
CODEC & SCALAR I2S MUX



A0	Function	A1	Function
0	NC_X Connected to COM_X	0	NC_Y Connected to COM_Y
1	NO_X Connected to COM_X	1	NO_Y Connected to COM_Y

Notes:
1. X = 1 or 2
2. Y = 3 or 4

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Asia Vital Components Co., Ltd.		
Title: P47 RESERVED		
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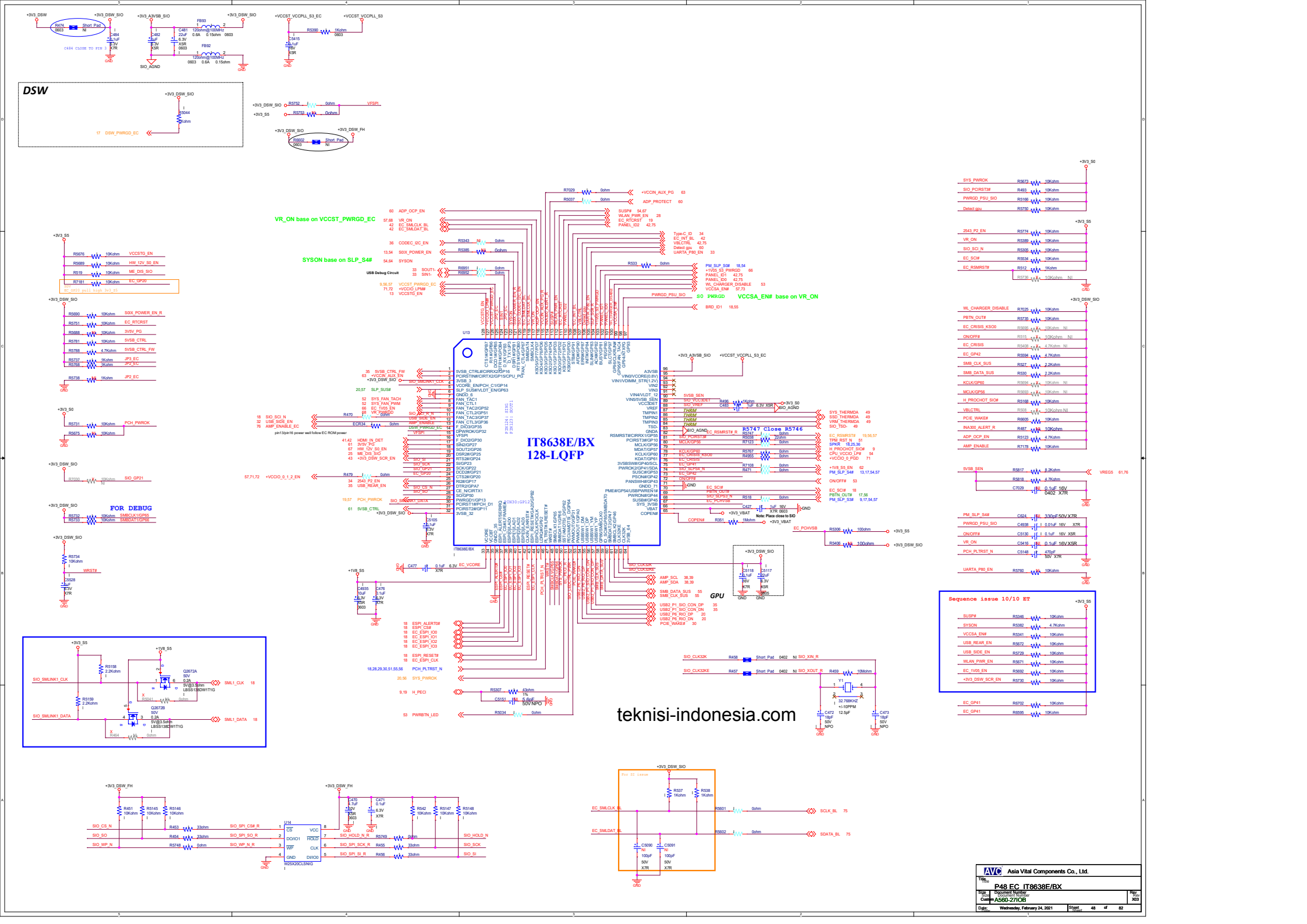
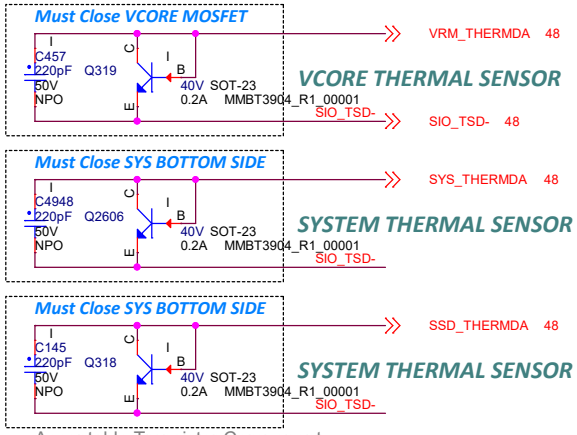

DSW
VR_ON base on VCCST_PWRGD_EC
SYSON base on SLP_S4#
S0 PWRGD
VCCSA_EN# base on VR_ON
IT8638E/BX
128-LQFP
U13
FOR DEBUG
GPU
Sequence issue 10/10 ET
R5747 Close R5746
teknisi-indonesia.com
Asia Vital Components Co., Ltd.
P48 EC_IT8638E/BX
A560-27IOB
Wednesday, February 24, 2021

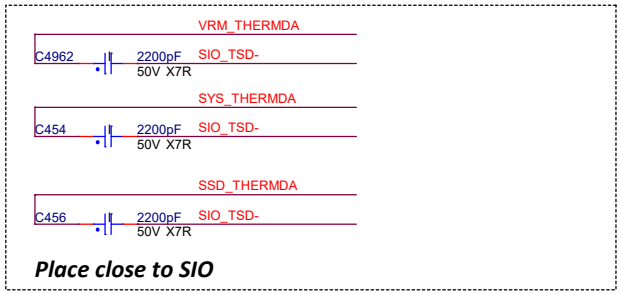
eSIO SETUP

THERMAL SENSOR



Acceptable Transistor Component
ST Micro: MMBT3904
ON Semiconsuctor: MMBT3904LT1
Fairchild Semiconductor: MMBT3904FSCT

CAD NOTE : Place MLCC Close to Thermal Diode



AVC Asia Vital Components Co., Ltd.		
Title: P49 eSIO_SETUP		
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Asia Vital Components Co., Ltd.		
Title: P50 RESERVED		
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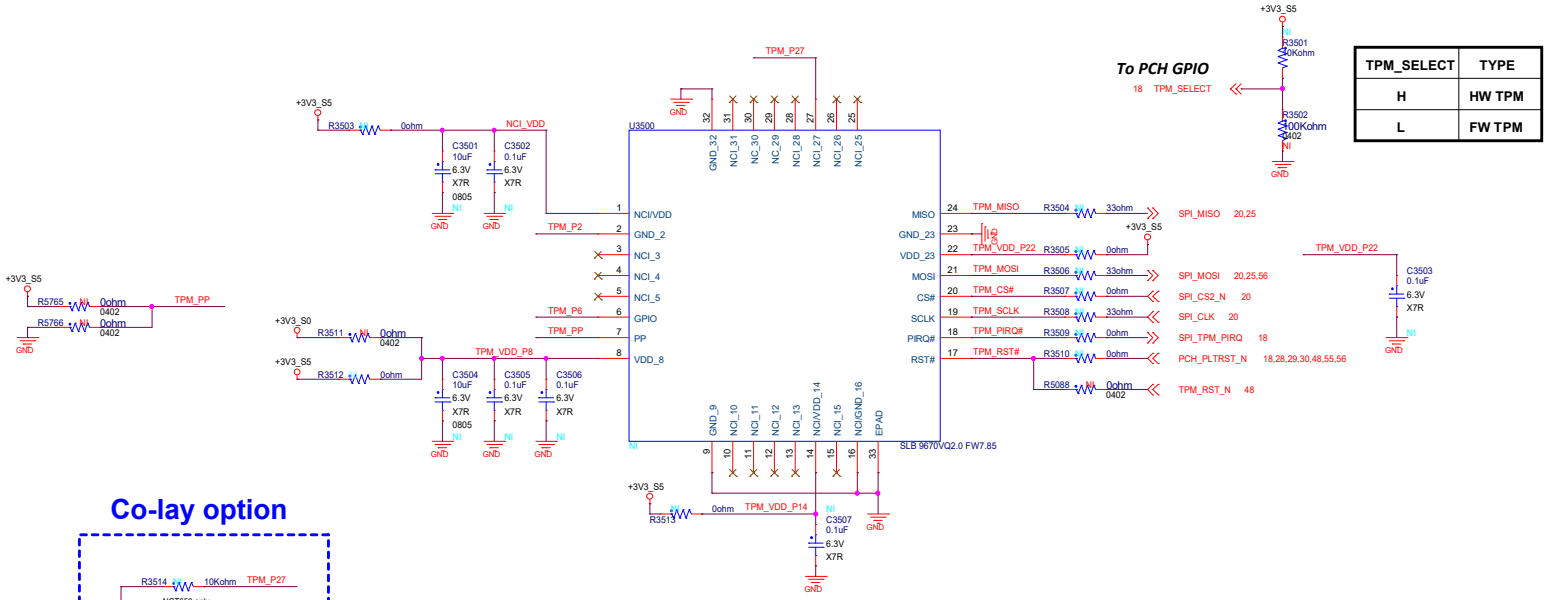
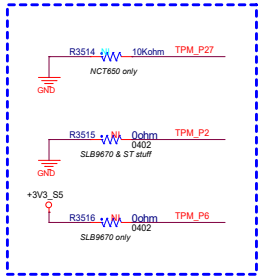
TPM 2.0



TPM_SELECT	TYPE
H	HW TPM
L	FW TPM

Co-lay option



		nuvoTon	Infineon	ST
TPM_P27				
TPM_P2				
TPM_P6				

Asia Vital Components Co., Ltd.	
Title: P51 TPM2.0	
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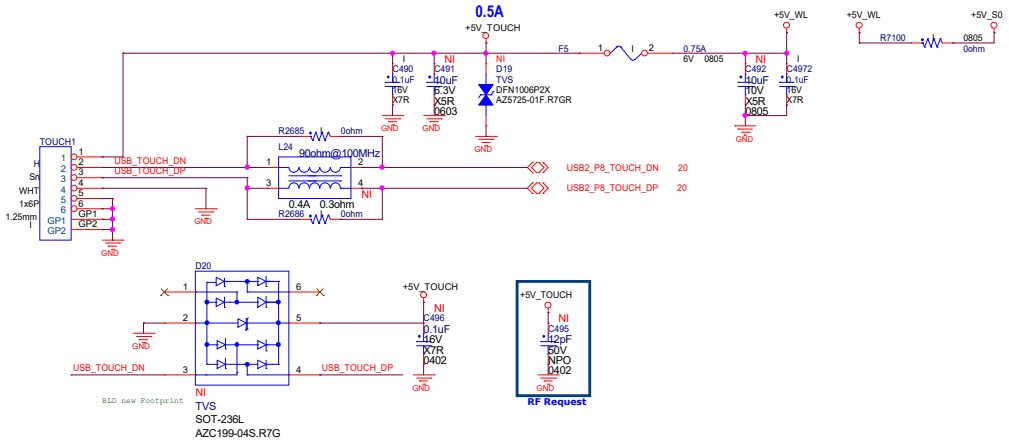
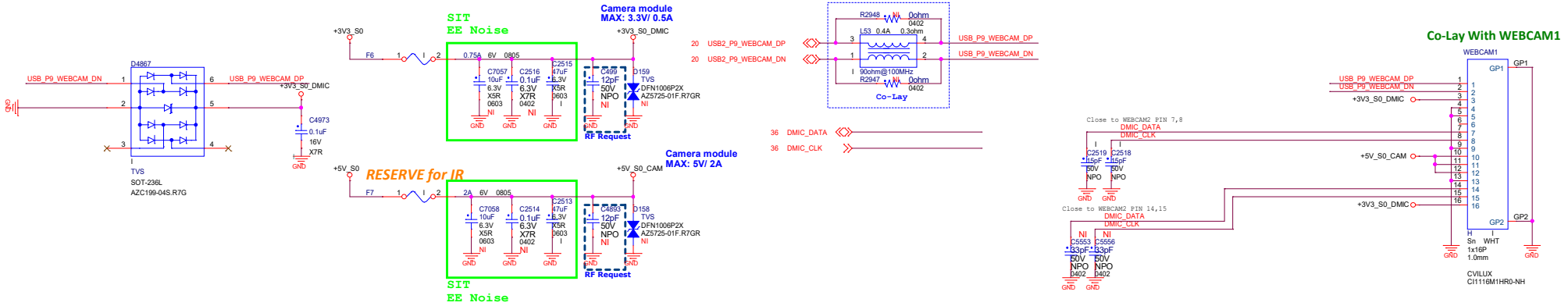
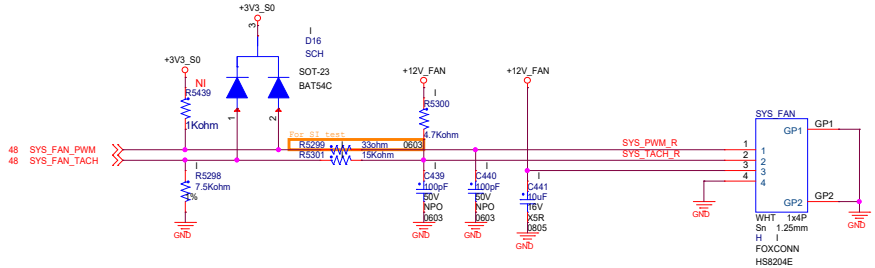
Touch

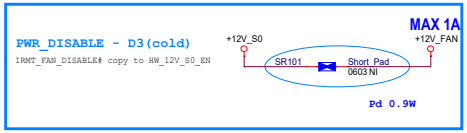


CAMERA (2D / IR)



SYS_FAN





Asia Vital Components Co., Ltd.			
Title: P52 TOUCH/ WebCAM/ DMIC			
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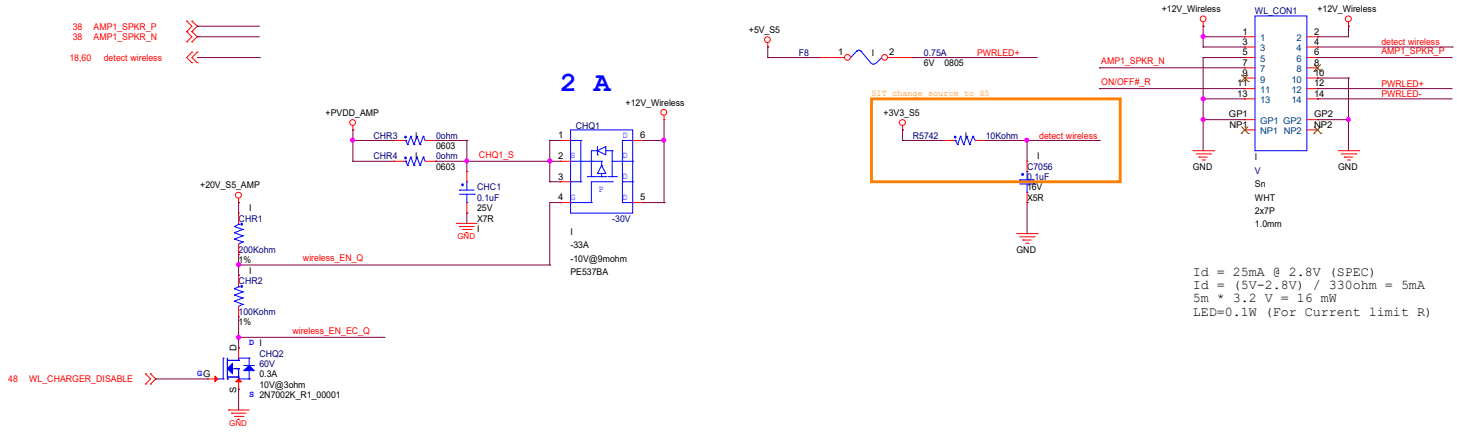
WIRELESS CHARGER CONN

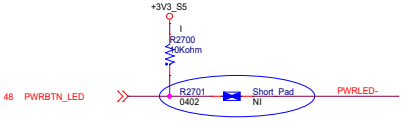


Pin #	Name	Description
1	+12V	POWER
2	+12V	POWER
3	+12V	POWER
4	GND	GND
5	GND	GND
6	AMP1_SPKR_L+	Analog output L+
7	AMP1_SPKR_L-	Analog output L-
8	AMP1_SPKR_R-	Analog output R-
9	AMP1_SPKR_R+	Analog output R+
10	GND	GND

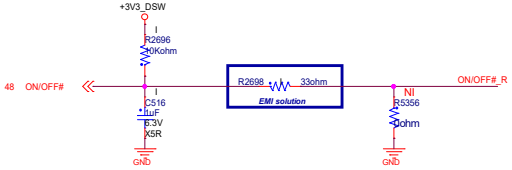
Id = 25mA @ 2.8V (SPEC)
Id = (5V-2.8V) / 330ohm = 5mA
5m * 3.2 V = 16 mW
LED=0.1W (For Current limit R)

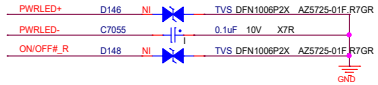
NO.	Input Power(W)	
	no RX	RX=0A
S1	0.103	1.710
S2	0.131	1.840
Spec	<1W	<3W

Power Button LED



Power LED	
S0	LED is on steady WHT
S1 / S3	LED Blinks (1Hz/s)
S4 / S5	LED OFF





AVC	Asia Vital Components Co., Ltd.	
Title	P53 WIRELESS CHARG/PWRBTN/LED	
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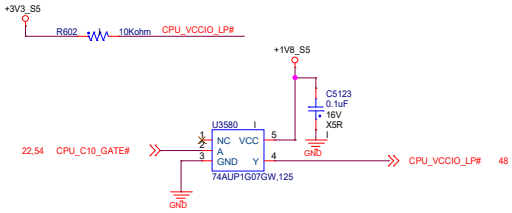
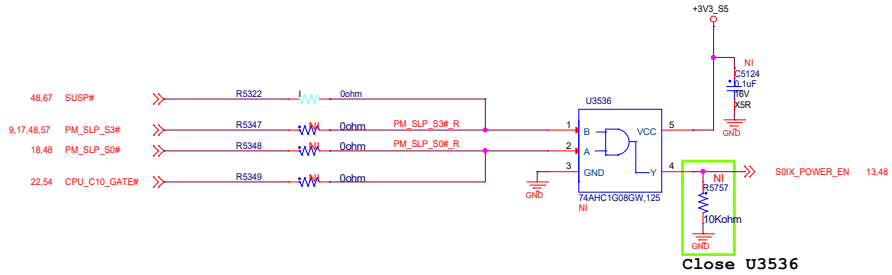
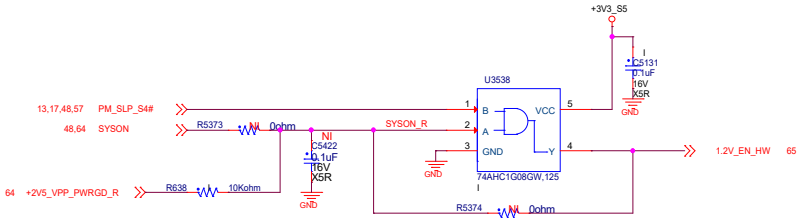
MODERN STANDBY/CEC







AVC Asia Vital Components Co., Ltd.		
Title: P54 CEC/Modern Standby		
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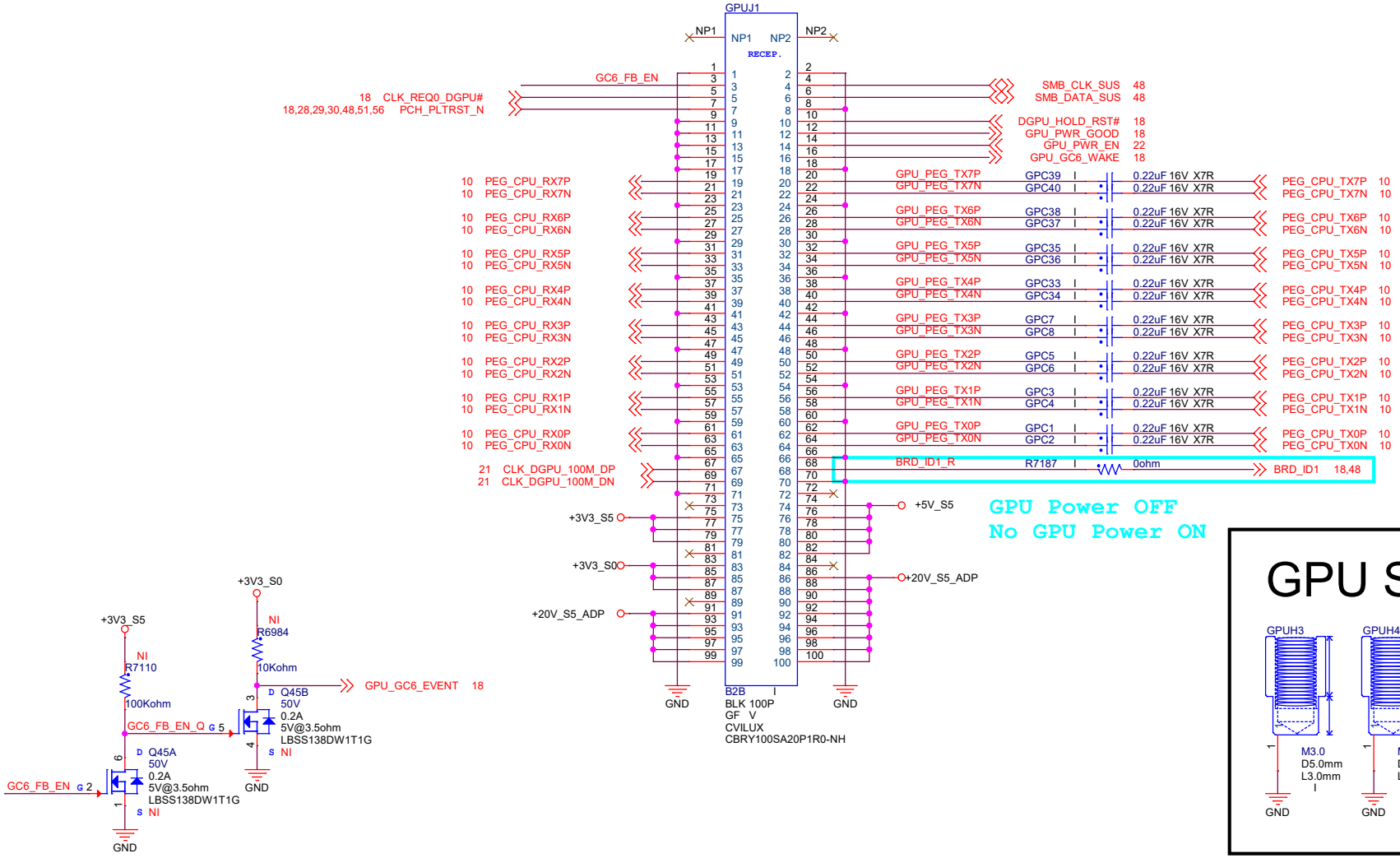
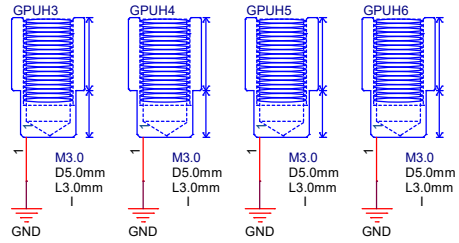
GPU CONN



GPU Stand Off



AVC Asia Vital Components Co., Ltd.		
Title: P55 GPU PCIE		
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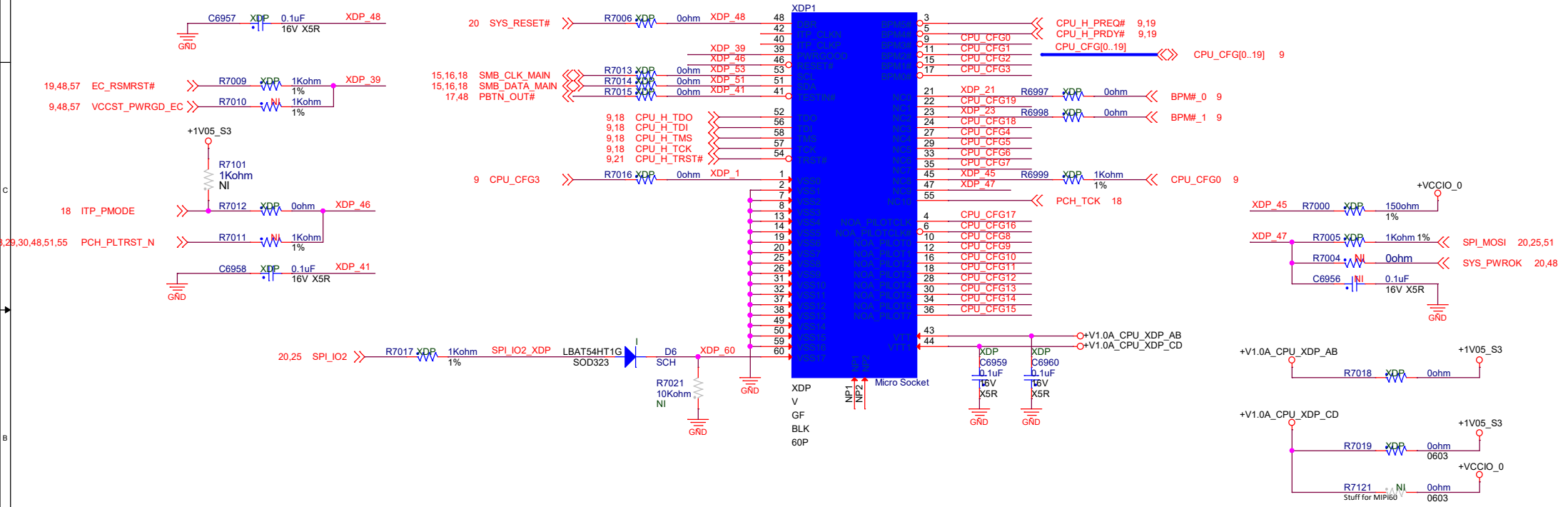
XDP CONN.



Asia Vital Components Co., Ltd.			
Title: P56 XDP			
Size: B	Document Number: A560-27IOB		Rev: X03
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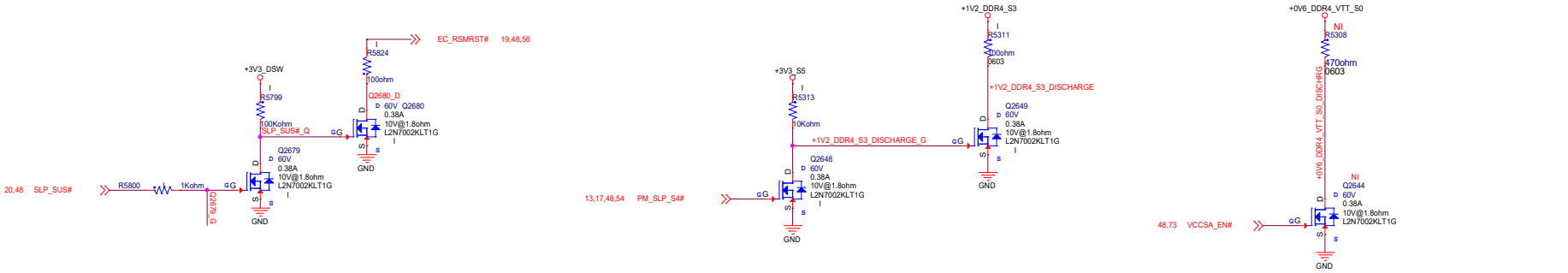

SDV
Change Power Seqence
Bleed off

AVC Asia Vital Components Co., Ltd.			
Title: P57 BLEED OFF			
Size: C	Document Number: A560-2710B		Rev: X03
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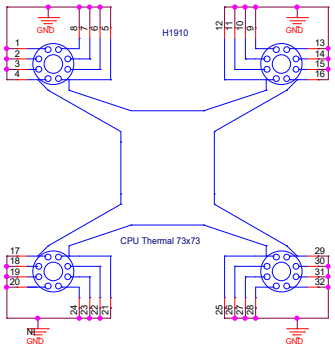
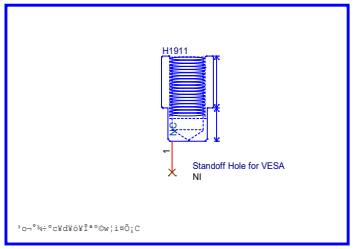
FIDUCIAL MARK

CPU HEATSINK HOLE





LABEL

AML LABEL1

BIOS 10x10mm

I

PCB

PCB1

PCB

PCB

I

BOM-METAL

XU_E

Socket

CPU (Metal Part)

I

BAR CODE Label

LB6

PN LABEL

8S Barcode 43x9mm

I

FRU Label

LB5

PN LABEL

FRU BARCODE 42x13mm

I

LAN Label

LB7

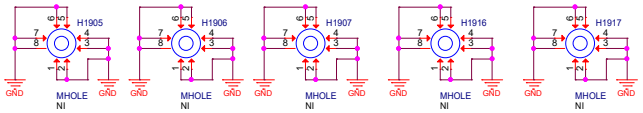
PN LABEL

MAC Address 31x5.73mm

I

BLD Label

SCREW



FAN SCREW & STAND-OFF

AVC Asia Vital Components Co., Ltd.		
Title: P58 SPARE PARTS		
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RESERVED

Asia Vital Components Co., Ltd.		
Title: P59 RESERVED		
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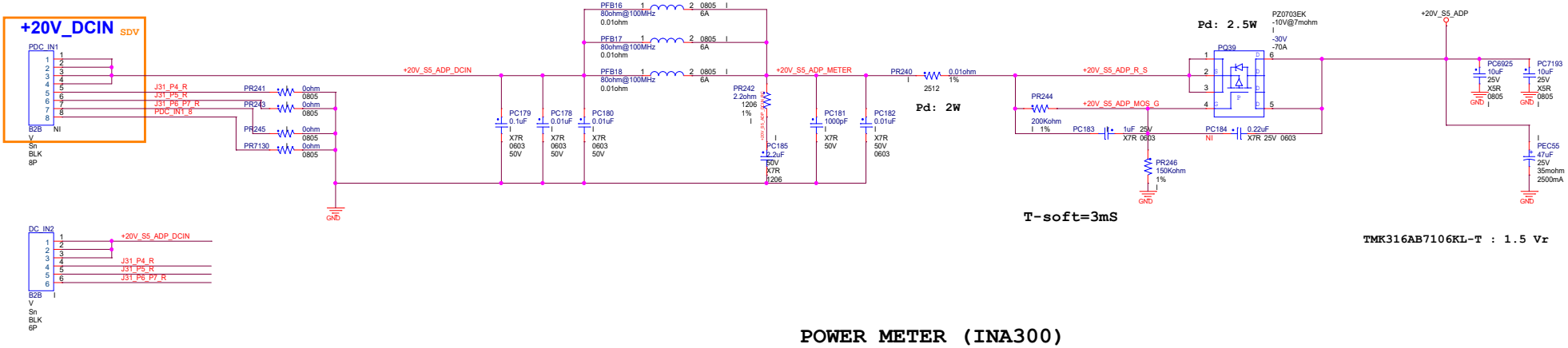
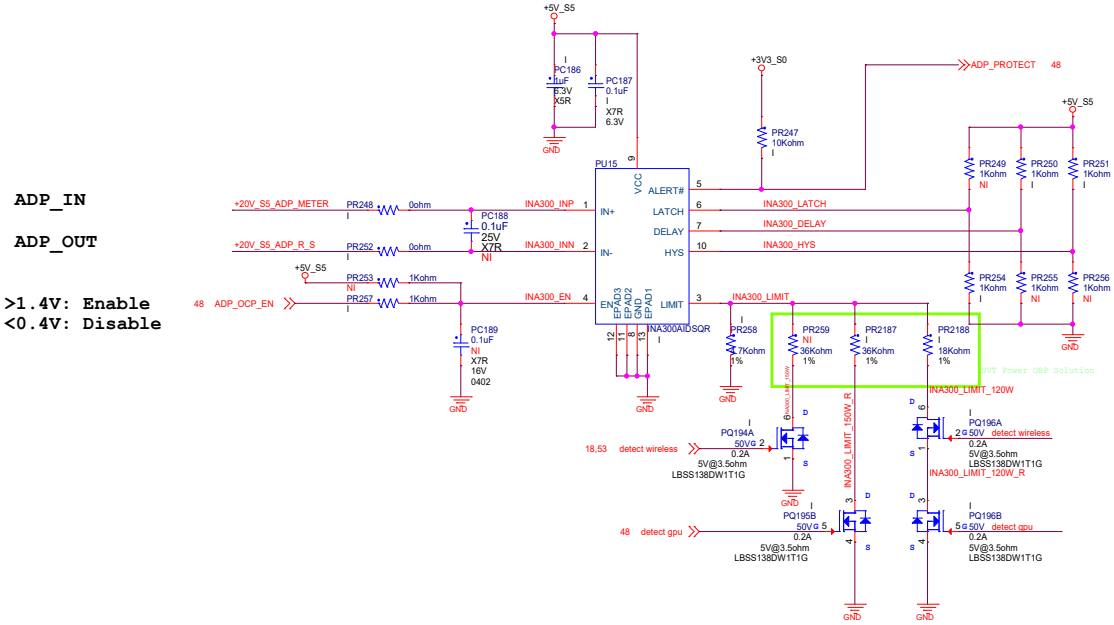


POWER METER (INA300)



DELAY
10us: Float
50us: GND
100us: VCC (default)

HYS
2mV: Float
4mV: GND
8mV: VCC (default)

LATCH:
OFF: GND (default)
ON: VCC

120W : 6 AAction
(Calculate 6.075A) Action ALERT
150W : 7.5 AAction
(Calculate 7.558A) Action ALERT
170W : 8.5 A Action
(Calculate 8.55A) Action ALERT

detect gpu	detect wireless	OBP
0	0	170W W/G
0	1	150W W/N
1	0	150W N/G
1	1	120W N/N

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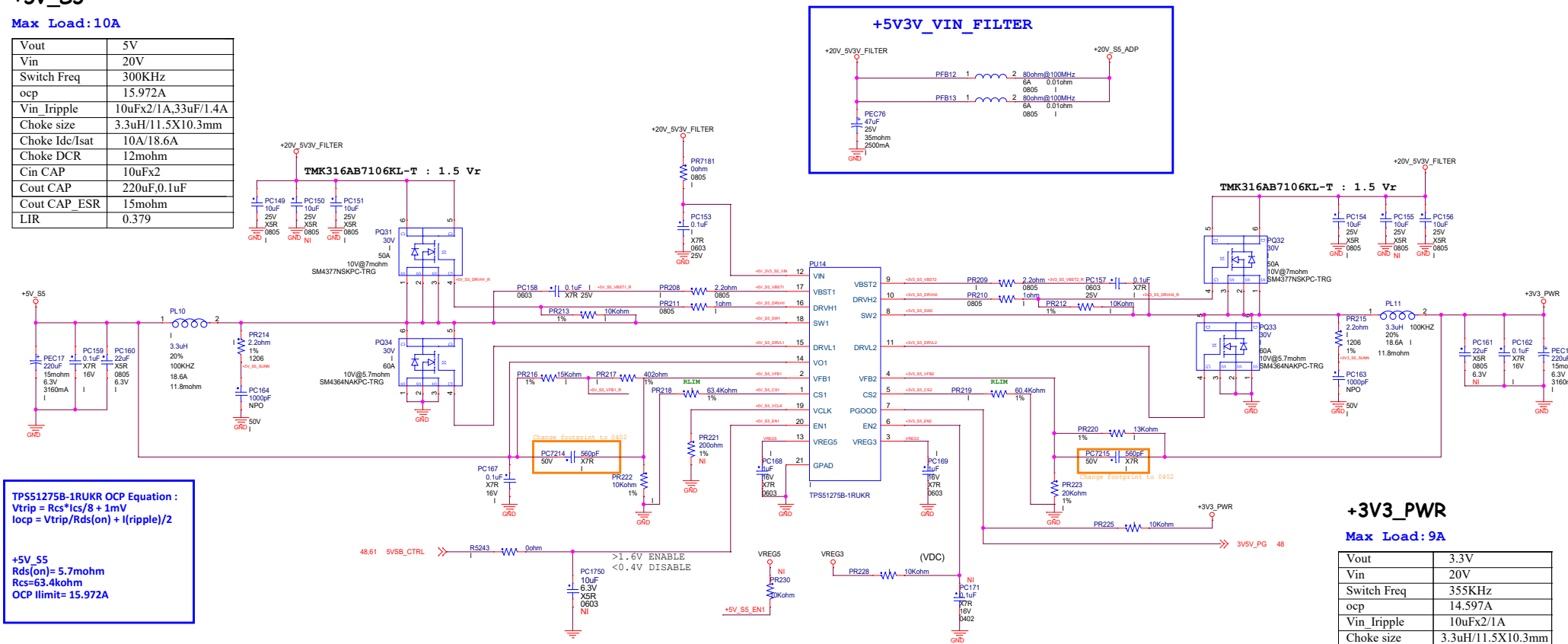
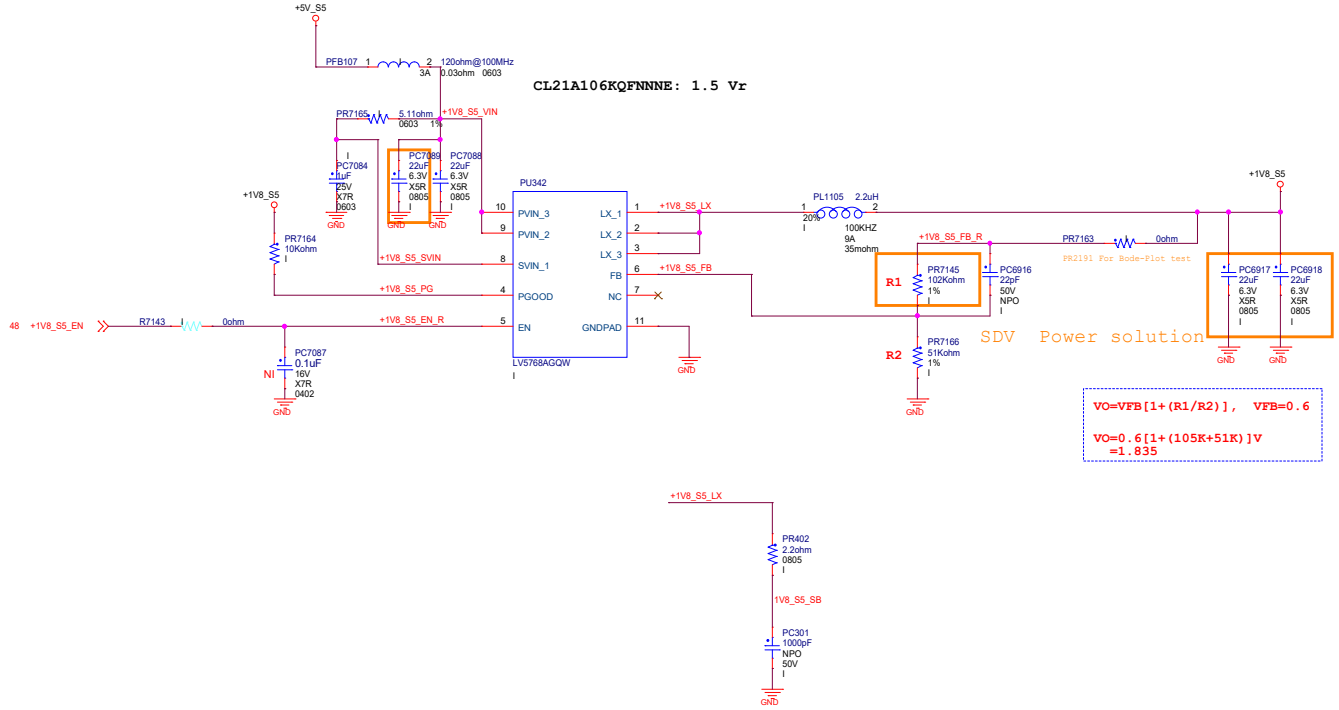
+5V_S5

Max Load:10A

Vout	5V
Vin	20V
Switch Freq	300KHz
ocp	15.972A
Vin_Iripple	10uFx2/1A,33uF/1.4A
Choke size	3.3uH/11.5X10.3mm
Choke Idc/Isat	10A/18.6A
Choke DCR	12mohm
Cin CAP	10uFx2
Cout CAP	220uF,0.1uF
Cout CAP_ESR	15mohm
LIR	0.379



+1V8_S5



Max Load:2A **CONVERTER**

Vout	1.8V
Vin	5V
Switch Freq	1MHz
ocp	6A (Fixed)
Vin_Iripple	10uF/1A
Choke size	2.2uH / 5.5x5.0mm
Choke Idc/Isat	
Choke DCR	35mohm
Cin CAP	22uF
Cout CAP	10uF x2
Cout CAP_ESR LIR	

Title	P62 +1V8_S5	
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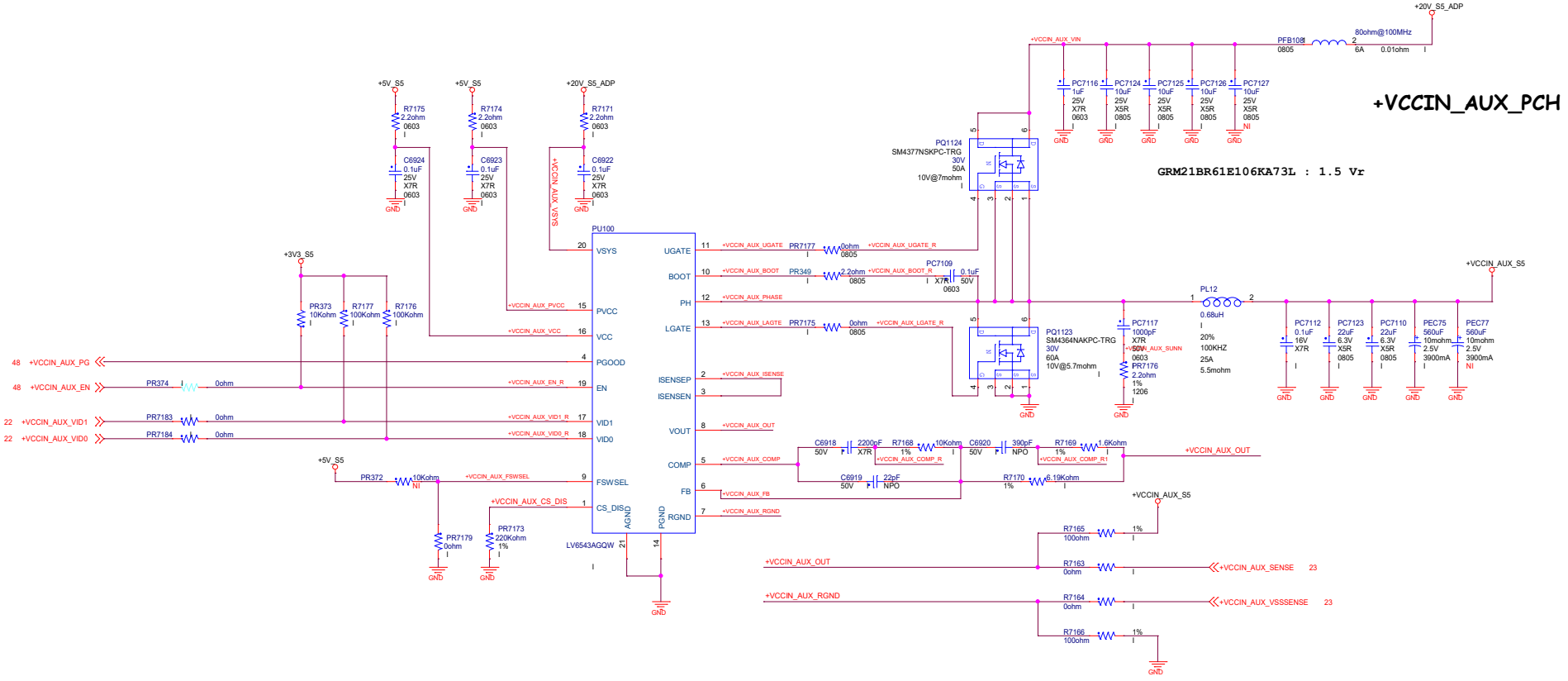
Imax:11.2A

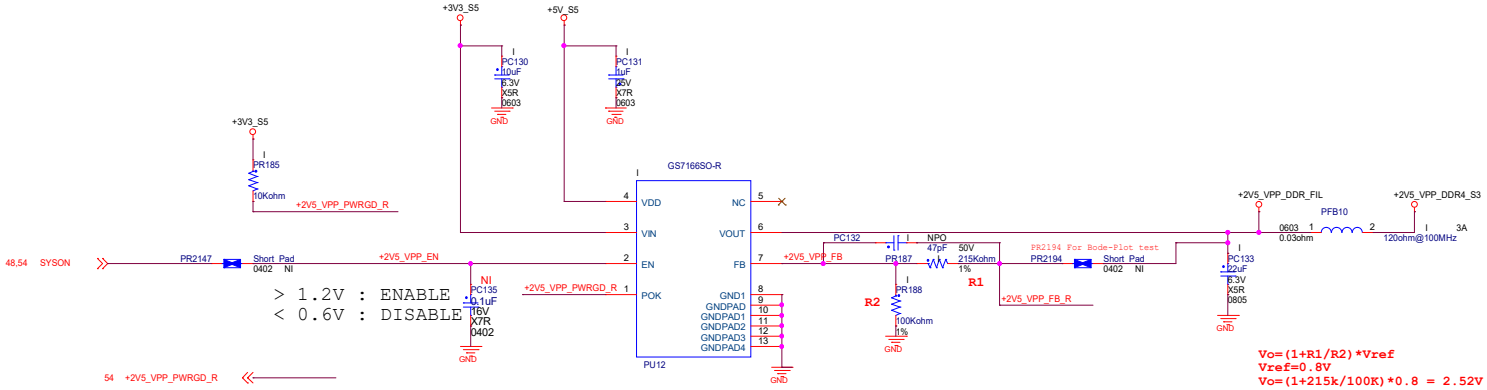
Vout	1.8V
Vin	20V
Switch Freq	400KHz
ocp	17.2A
Vin_Iripple	10uFx2/1A
Choke size	0.68uH/7.3X6.8mm
Choke Idc/Isat	15.5A/25A
Choke DCR	5.5mohm
Cin CAP	10uFX3
Cout CAP	560uF X1
Cout CAP_ESR	10mohm
LIR	0.537



Title	P63 +VCCIN_AUX		
Size C	Document Number A560-27IOB		Rev X03
Date: Wednesday, February 24, 2021		Sheet 63 of 82	

+2V5_VPP_DDR4_S3

Vin: +3V3
Vout: +2V5
Imax: 1A
OCP: 4A
Pd: 0.8W
Rja: 75
EN ON > 1.2V
EN OFF <0.6V



Pd: 1.33W

Vo=(1+R1/R2)*Vref
Vref=0.8V
Vo=(1+215k/100K)*0.8 = 2.52V

Title	P64 +2V5_VPP_DDR4_S3		
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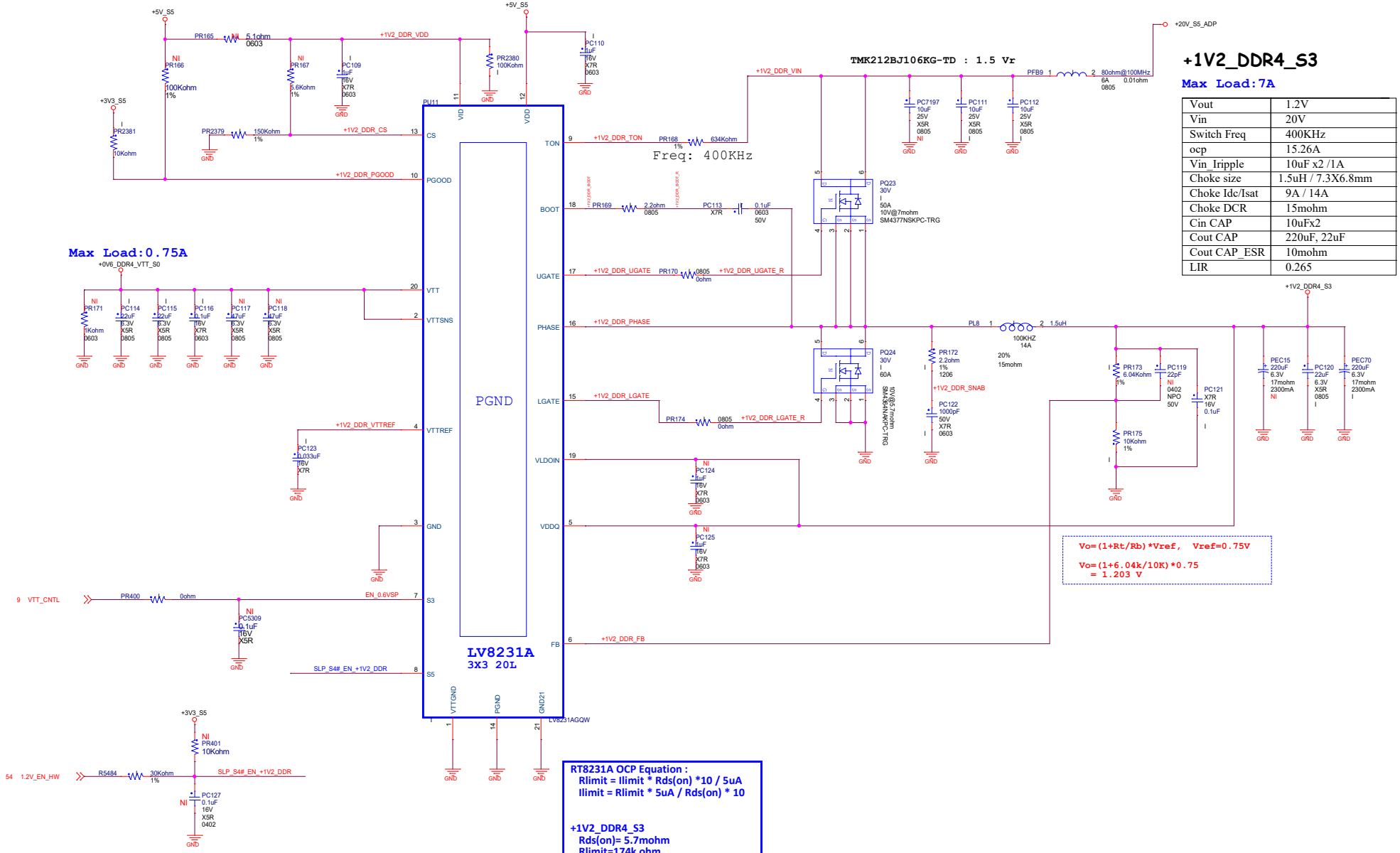

Vout	1.2V
Vin	20V
Switch Freq	400KHz
ocp	15.26A
Vin_Iripple	10uF x2 /1A
Choke size	1.5uH / 7.3X6.8mm
Choke Idc/Isat	9A / 14A
Choke DCR	15mohm
Cin CAP	10uFx2
Cout CAP	220uF, 22uF
Cout CAP_ESR	10mohm
LIR	0.265

VID and Reference Voltage Setting

VID	Reference Voltage (V)
High	0.675
Low	0.75

Title	P65 +1V2_DDR4_S3/+0V6_DDR4_VTT		
Size C	Document Number A560-27IOB		Rev X03
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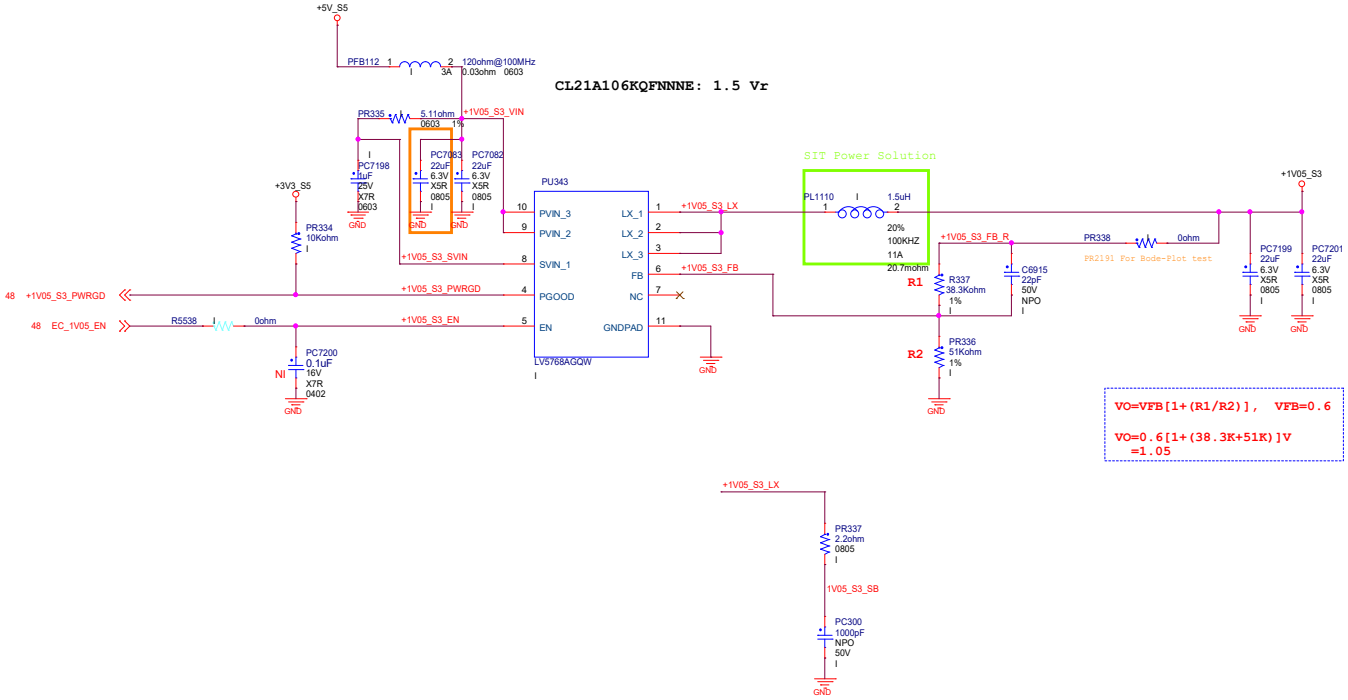
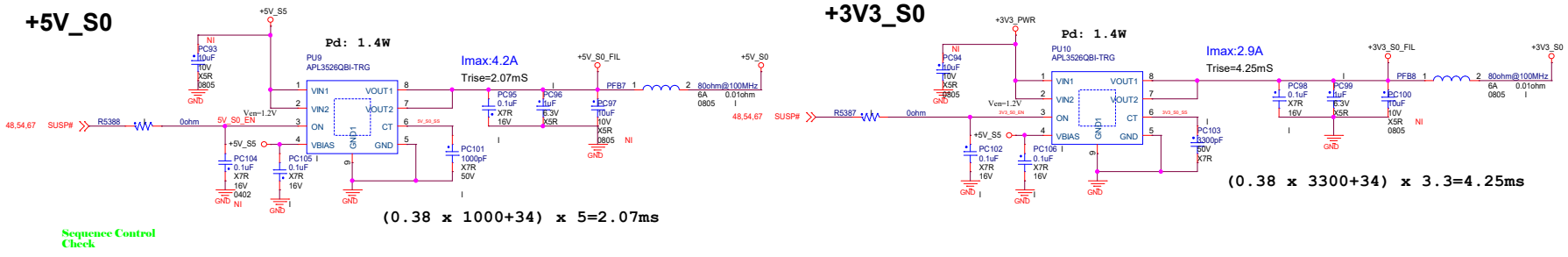
+1V05_S3

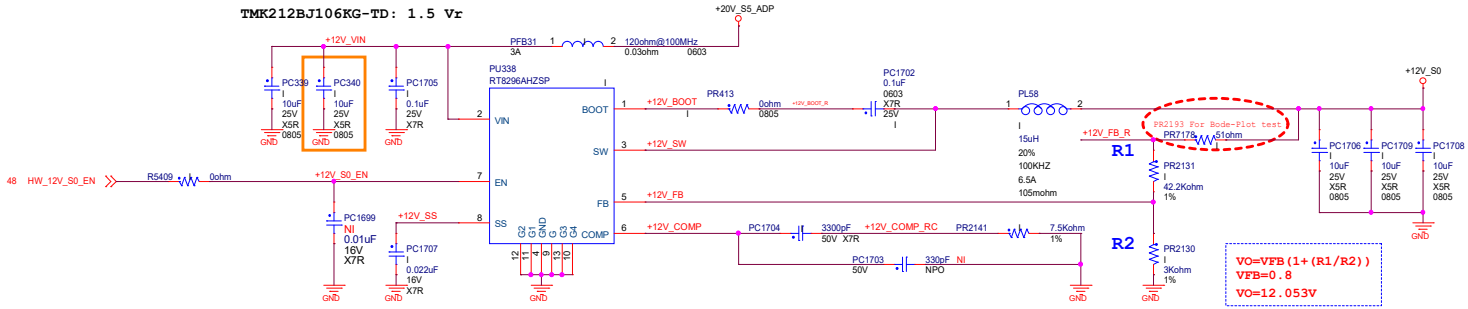


Max Load:3A **CONVERTER**

Vout	1.05V
Vin	5V
Switch Freq	1MHz
ocp	6A (Fixed)
Vin_Iripple	10uF/1A
Choke size	2.2uH / 5.5x5.0mm
Choke Idc/Isat	
Choke DCR	35mohm
Cin CAP	22uF
Cout CAP	22uF x2
Cout CAP_ESR LIR	

Title	P66 +1V05_S3	
Size C	Document Number A560-27IOB	Rev X03
Date: Thursday, March 04, 2021	Sheet 66 of 82	



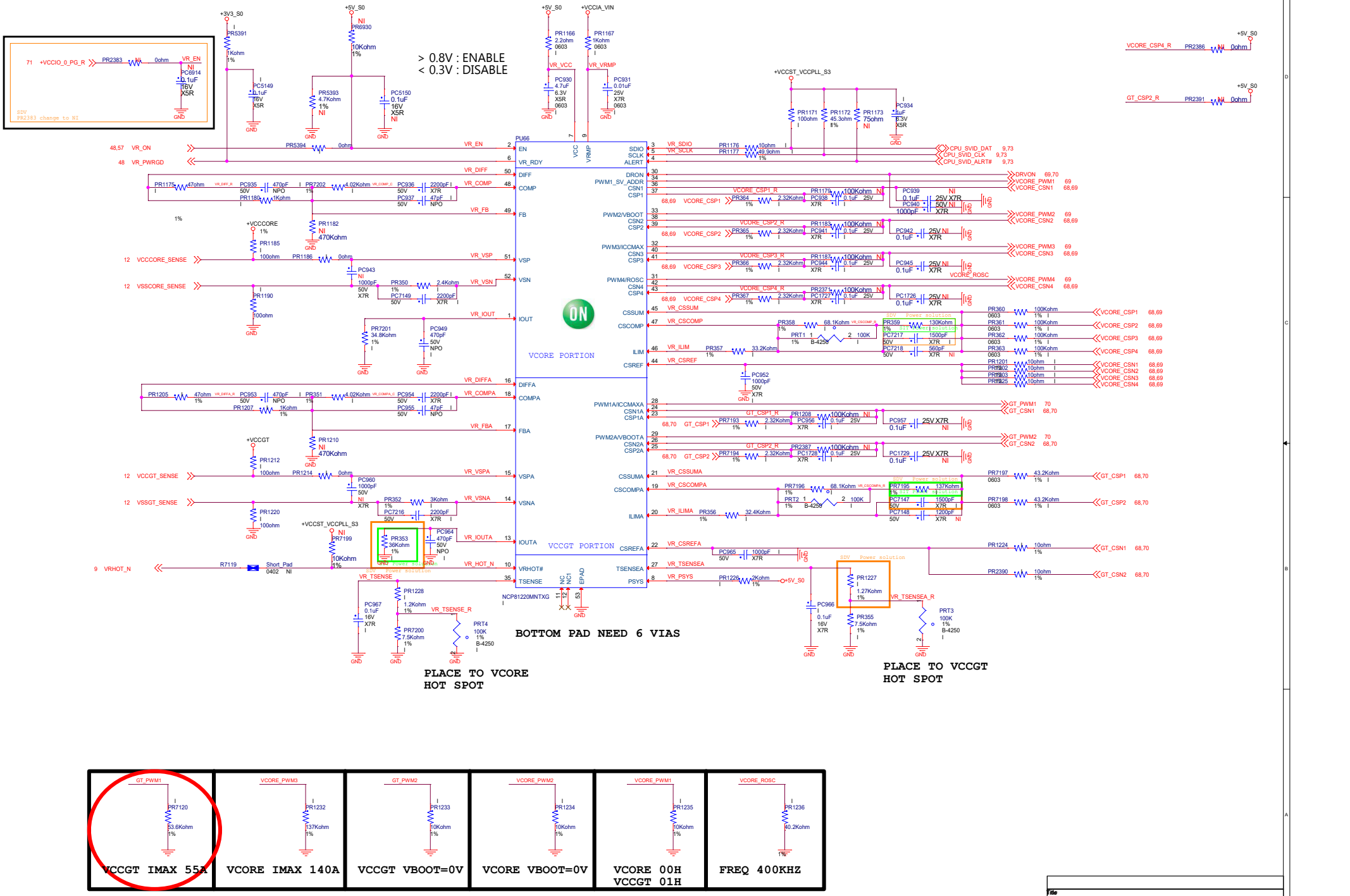


+12V_S0

Max Load:0.7A

Vout	12V
Vin	20V
Switch Freq	340KHz
ocp	5.1A
Vin_Iripple	10uF/1A
Choke size	15uH/7.6x6.8mm
Choke Idc/Isat	3A/6.5A
Choke DCR	105mohm
Cin CAP	10uF,0.1uF
Cout CAP	10uFx2
Cout CAP_ESR	
LIR	

Title: P67 +12V_S0/+5V/+3V3_S0		
Size: C	Document Number: A560-27IOB	Rev: X03
Date: Wednesday, February 24, 2021	Sheet 67 of 82	



Title	P68 +Vcore Controller		
Size C	Document Number A560-27IOB		Rev X03
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SDV
Power solution

+20V_S5_ADP → +VCCIA_VIN

PL67 0805 1 2 80ohm@100MHz 6A 0.01ohm
PL1111 0805 1 2 80ohm@100MHz 6A 0.01ohm
PL1112 0805 1 2 80ohm@100MHz 6A 0.01ohm

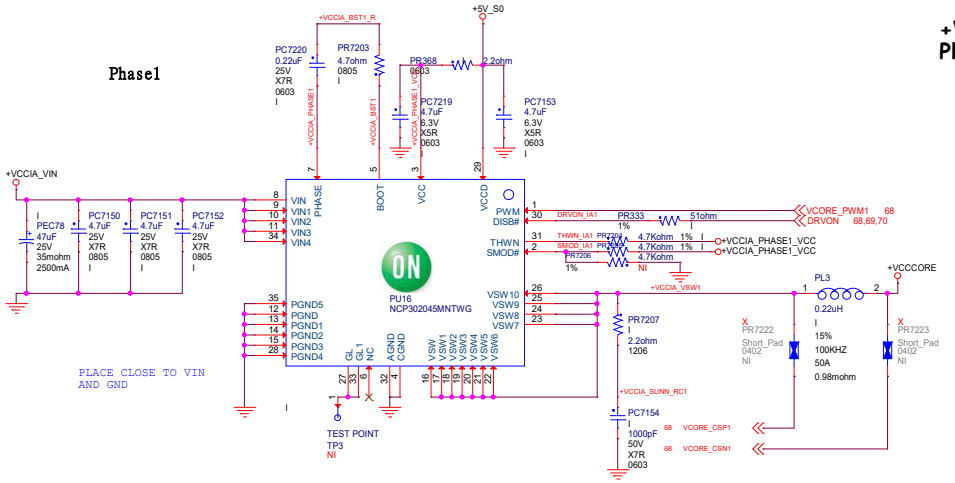
CL31B106KAHNNNE : 1.5 Vr

+VCORE
Phase 1~Phase 4

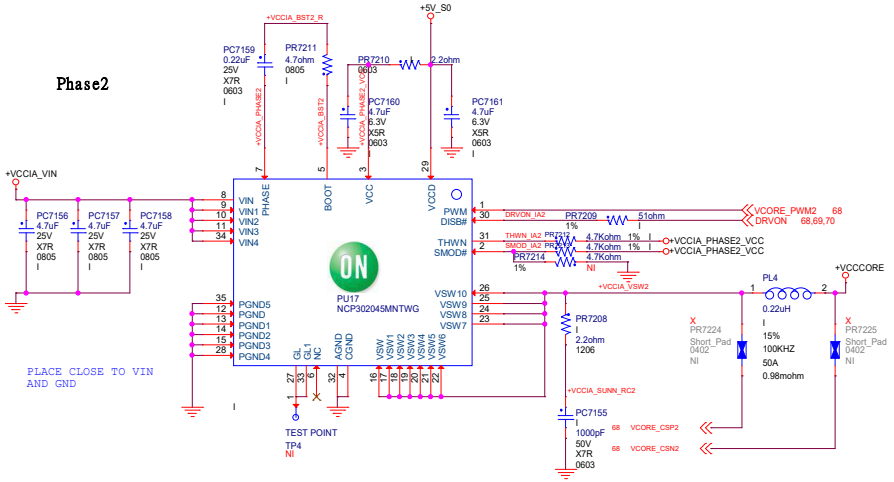
+VCORE
Vin:+20V
Vout:+VCORE
DC Loadline: 1.7mohm
ITDC: 100A
Imax:140A

Vout	Vcore
Vin	20V
Switch Freq	400KHz
minimum ocp	210A
Vin_Iripple	47uFx2/2.5A,10uFx10/1A
Choke size	0.3uH/11X7.3mm
Choke Idc/Isat	30A/60A
Choke DCR	1.05mohm
Cin CAP	47uFx2,10uFx10
Cout CAP	560uFx6
Cout CAP_ESR	10mohm x 6
LIR	

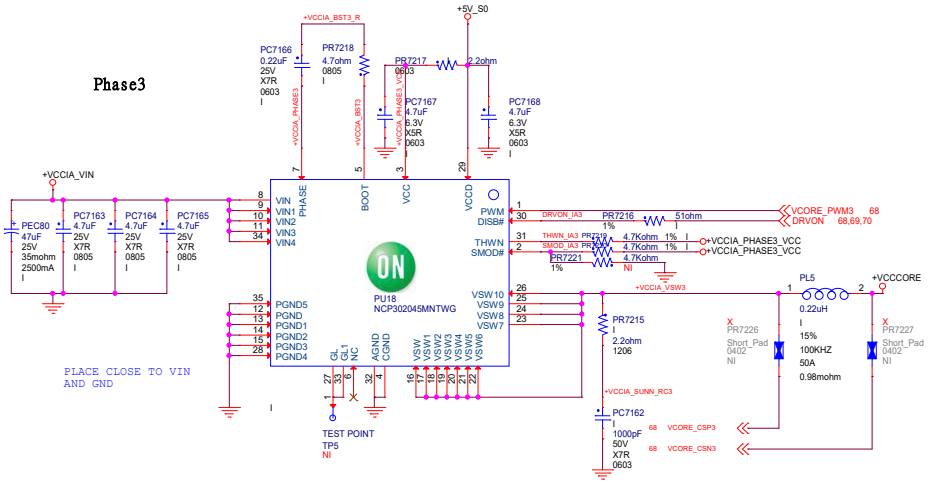
Phase1



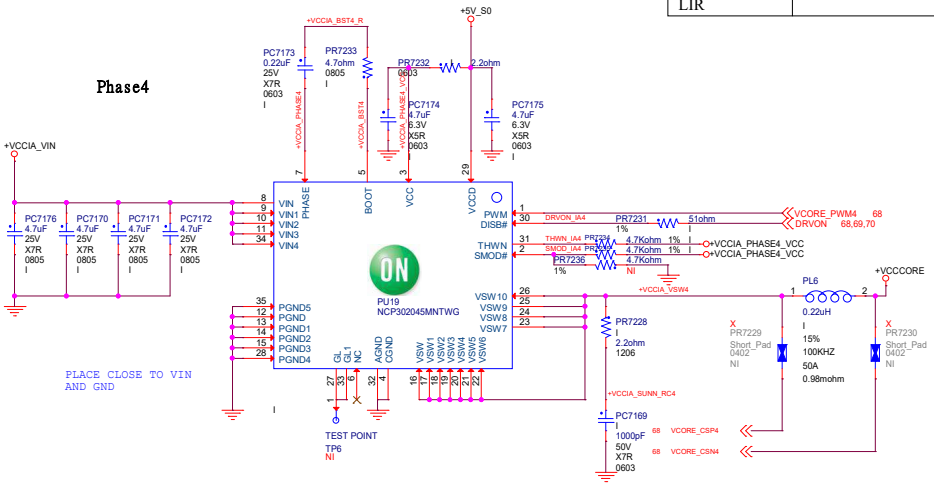
Phase2

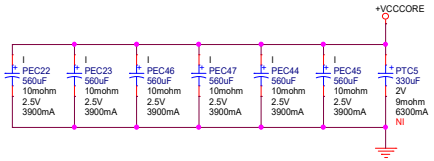


Phase3

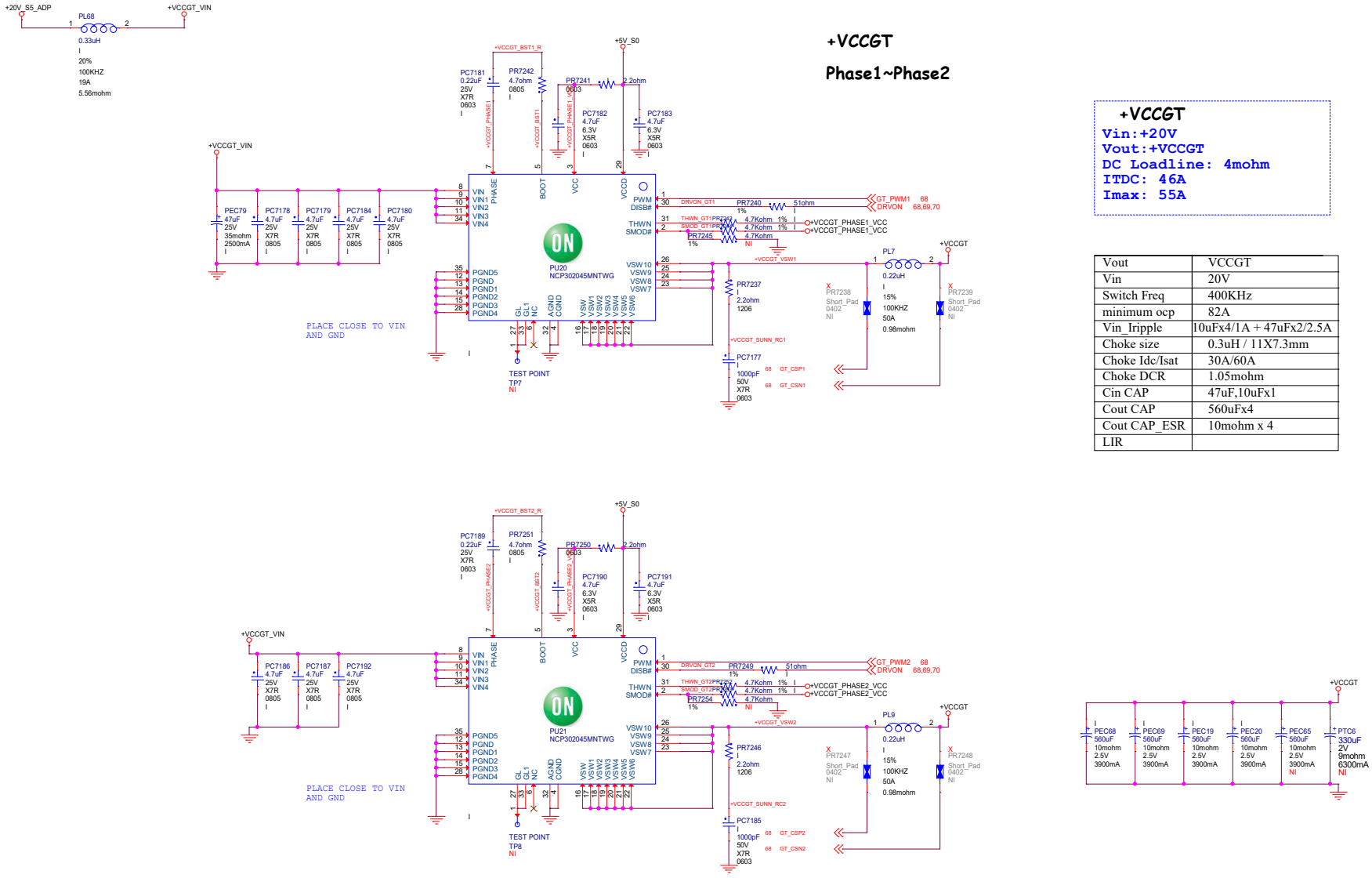


Phase4





Title	P69 +VCCIA Phase1~4 Output	
Size C	Document Number A560-27IOB	Rev X03
Date: Wednesday, February 24, 2021	Sheet 69 of 82	



Vout	VCCGT
Vin	20V
Switch Freq	400KHz
minimum ocp	82A
Vin_Iripple	10uFx4/1A + 47uFx2/2.5A
Choke size	0.3uH / 11X7.3mm
Choke Idc/Isat	30A/60A
Choke DCR	1.05mohm
Cin CAP	47uF,10uFx1
Cout CAP	560uFx4
Cout CAP_ESR	10mohm x 4
LIR	

Title:	P70 +VCCGT Phase1~2 OUT			
Size: C	Document Number: A560-27IOB			Rev: X03
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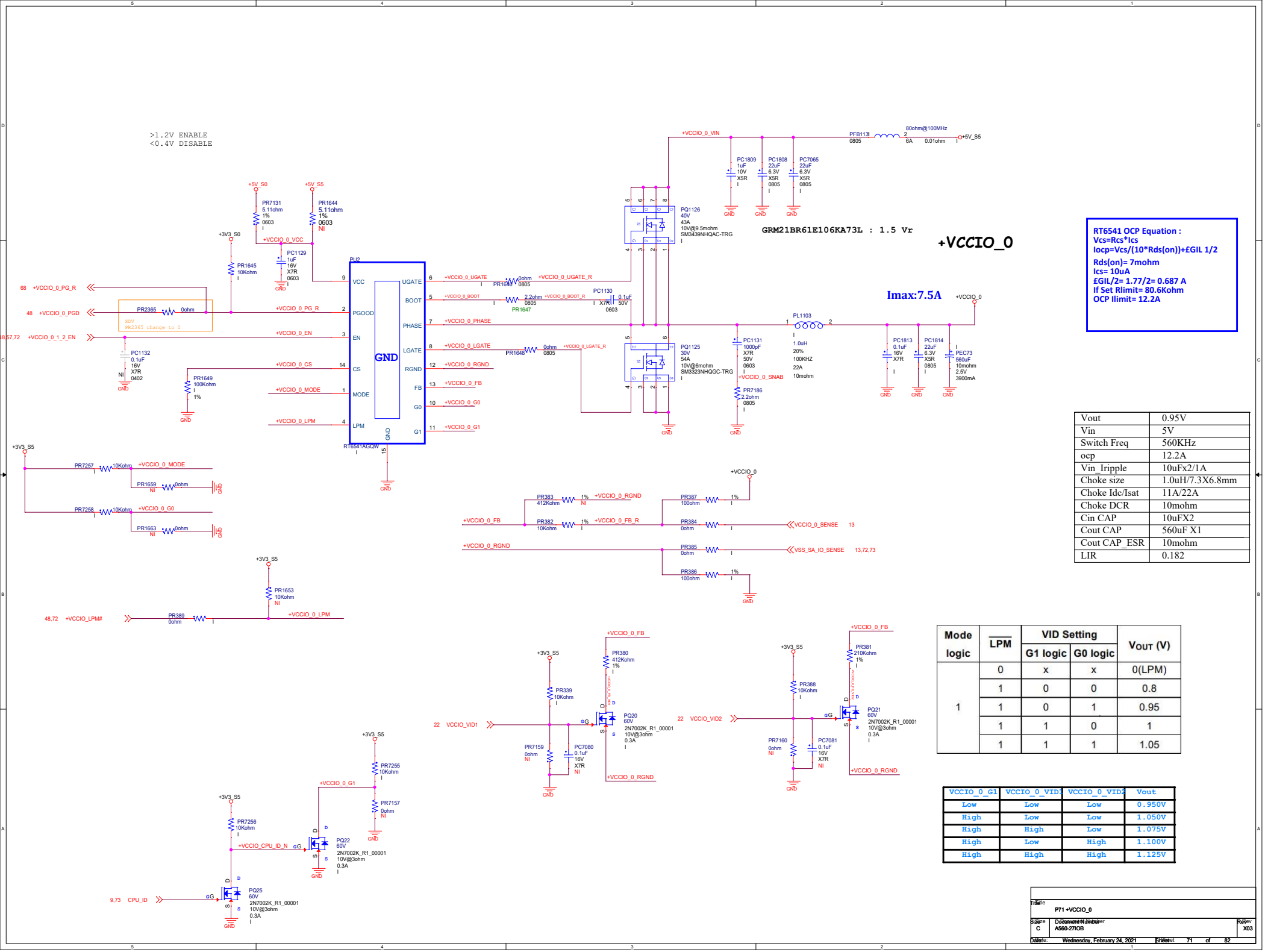

Vout	0.95V
Vin	5V
Switch Freq	560KHz
ocp	12.2A
Vin_Iripple	10uFx2/1A
Choke size	1.0uH/7.3X6.8mm
Choke Idc/Isat	11A/22A
Choke DCR	10mohm
Cin CAP	10uFX2
Cout CAP	560uF X1
Cout CAP_ESR	10mohm
LIR	0.182

Mode logic	$\overline{LPM}$	VID Setting		VOUT (V)
		G1 logic	G0 logic	
1	0	x	x	0(LPM)
	1	0	0	0.8
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05

VCCIO_0_G1	VCCIO_0_VID1	VCCIO_0_VID2	Vout
Low	Low	Low	0.950V
High	Low	Low	1.050V
High	High	Low	1.075V
High	Low	High	1.100V
High	High	High	1.125V

Title	P71 +VCCIO_0		
Size C	Document Number A560-27IOB		Rev X03
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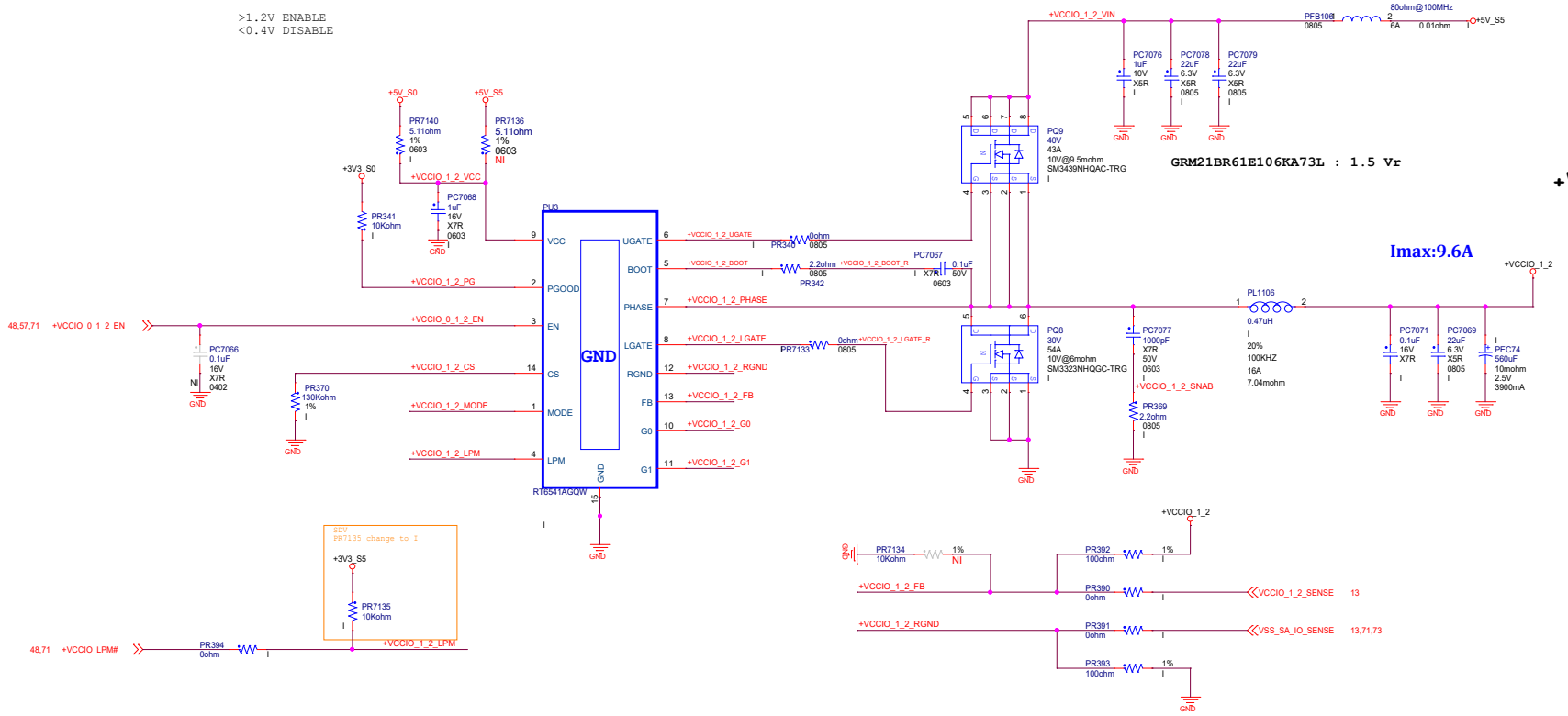

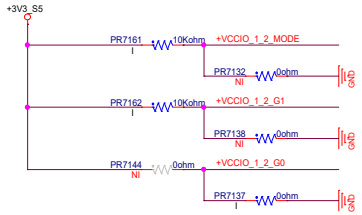

Mode logic	$\overline{LPM}$	VID Setting		V_{OUT} (V)
		G1 logic	G0 logic	
1	0	x	x	0(LPM)
	1	0	0	0.8
	1	0	1	0.95
	1	1	0	1
	1	1	1	1.05

Vout	1V
Vin	5V
Switch Freq	560KHz
ocp	15.8A
Vin_Iripple	10uFx2/1A
Choke size	0.47uH/5.7X5mm
Choke Idc/Isat	12A/16A
Choke DCR	7.04mohm
Cin CAP	10uFX2
Cout CAP	560uF X1
Cout CAP_ESR	10mohm
LIR	0.316

RT6541 OCP Equation :
Vcs=Rcs*Ics
Iocp=Vcs/(10*Rds(on))+£GIL 1/2

Rds(on)= 7mohm
Ics= 10uA
£GIL/2= 1.77/2= 1.519 A
If Set Rlimit= 100Kohm
OCP Ilimit= 15.8A

Title: P72 +VCCIO_1_2			
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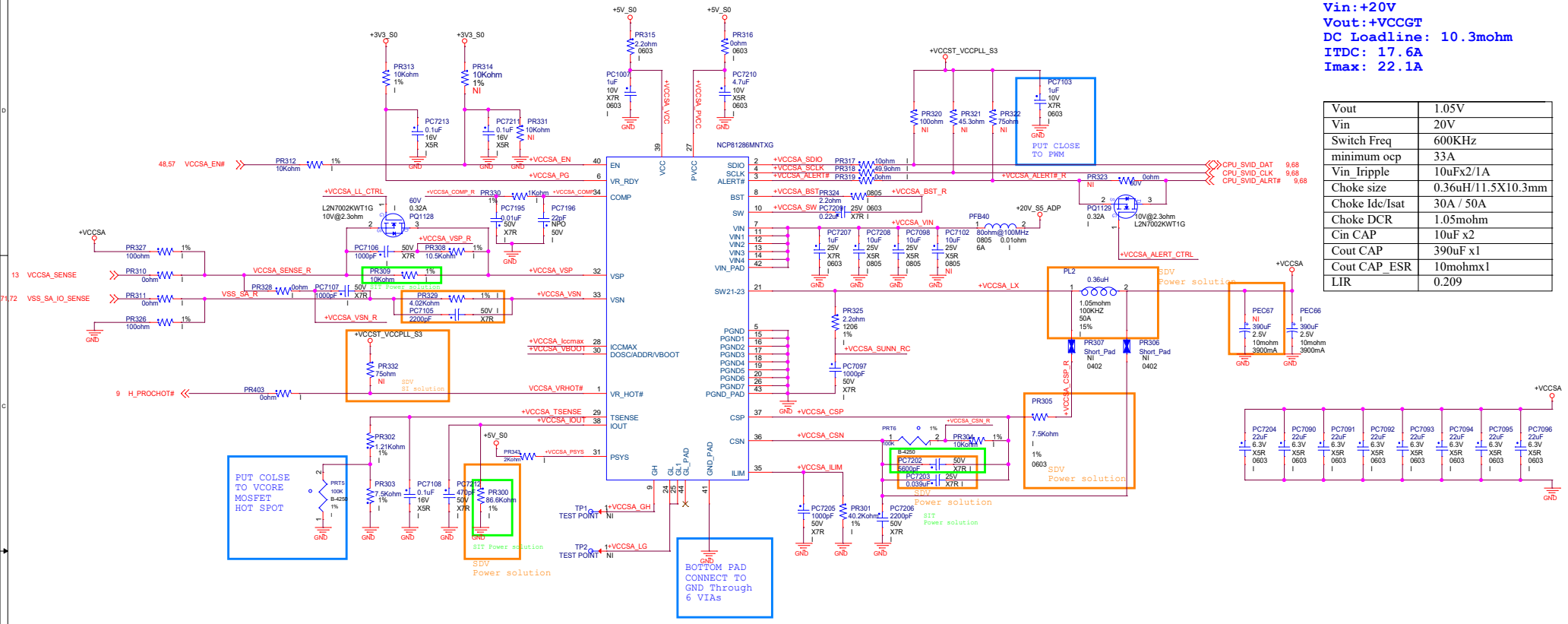
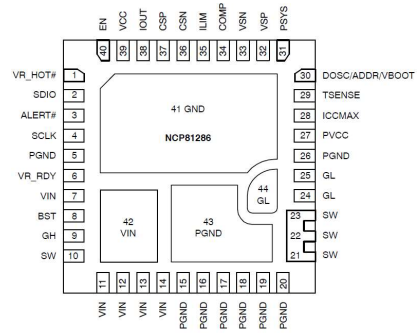
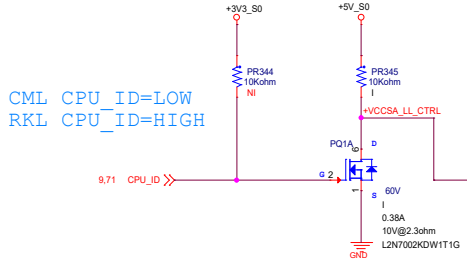
+VCCSA

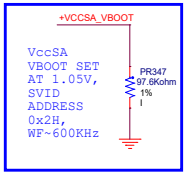
Vin:+20V
Vout:+VCCGT
DC Loadline: 10.3mohm
ITDC: 17.6A
Imax: 22.1A

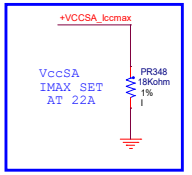
Vout	1.05V
Vin	20V
Switch Freq	600KHz
minimum ocp	33A
Vin_Iripple	10uFx2/1A
Choke size	0.36uH/11.5X10.3mm
Choke Idc/Isat	30A / 50A
Choke DCR	1.05mohm
Cin CAP	10uF x2
Cout CAP	390uF x1
Cout CAP_ESR	10mohmx1
LIR	0.209











Title	P73 +VCCSA
Size	C
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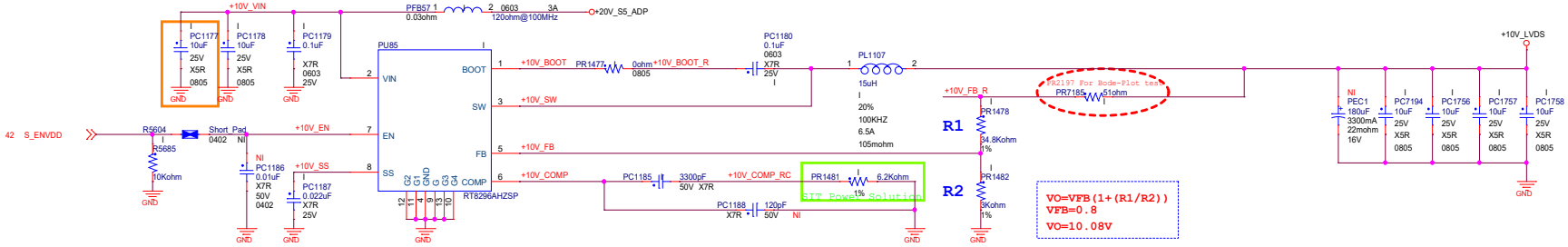
+10V_LVDS

Max Load:2.0A

Vout	10V
Vin	20V
Switch Freq	340KHz
ocp	5.1A
Vin_Iripple	10uF/1A
Choke size	15uH/7.6x6.8mm
Choke Idc/Isat	3A/6.5A
Choke DCR	105mohm
Cin CAP	10uF,0.1uF
Cout CAP	10uFx4
Cout CAP_ESR	
LIR	0.49

TMK212BJ106KG-TD : 1.5 Vr



Title	P74 +10V_LVDS		
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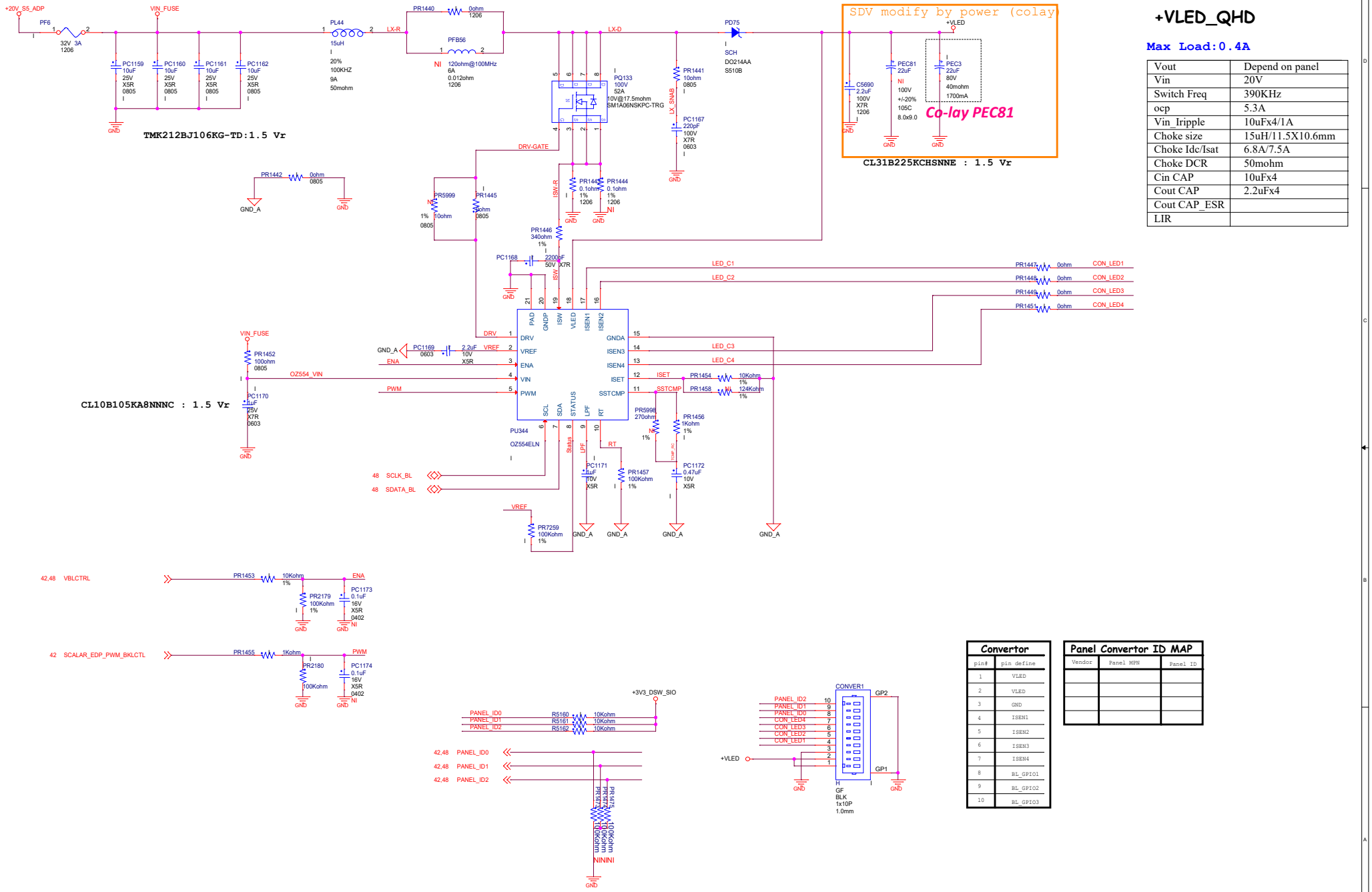
Date: Wednesday, March 03, 2021		Sheet 74 of 82	



+VLED_QHD

Max Load:0.4A

Vout	Depend on panel
Vin	20V
Switch Freq	390KHz
ocp	5.3A
Vin_Iripple	10uFx4/1A
Choke size	15uH/11.5X10.6mm
Choke Idc/Isat	6.8A/7.5A
Choke DCR	50mohm
Cin CAP	10uFx4
Cout CAP	2.2uFx4
Cout CAP_ESR	
LIR	

Convertor

pin#	pin define
1	VLED
2	VLED
3	GND
4	ISEN1
5	ISEN2
6	ISEN3
7	ISEN4
8	BL_GPIO1
9	BL_GPIO2
10	BL_GPIO3

Panel Convertor ID MAP

Vendor	Panel MPN	Panel ID

Asia Vital Components Co., Ltd.

Title: P75 +VLED

Size: C | Document Number: A560-27IOB | Rev: X03

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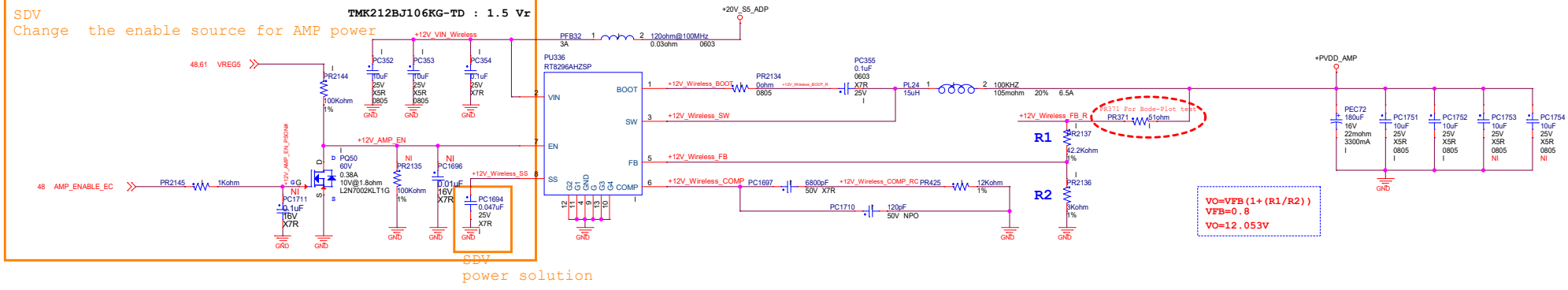
+PVDD_AMP

Max Load:2A

Vout	12V
Vin	20V
Switch Freq	340KHz
ocp	5.1A
Vin_Iripple	10uFx2/1A
Choke size	15uH/7.6x6.8mm
Choke Idc/Isat	3A/6.5A
Choke DCR	105mohm
Cin CAP	10uFx2,0.1uF
Cout CAP	10uFx3
Cout CAP_ESR	
LIR	

SDV
Change the enable source for AMP power

TMK212BJ106KG-TD : 1.5 Vr



SDV
power solution

Title	P76 +12V_Wireless		
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GPIO	PIN Name	AG465(Net Name) CFL-Z7	In/Out	Power well	STRP PIN	Internal PU/ PD	Default Termination @ PLTRST	External PU / PD	
				Primary Well Group A					
GPP_A0	GPP_A0/RCIN#/SPI_ALERT1#	KBRST_N	Fn 1	+3V3_SS				PU 10K to +3V3_SS (R5800)	
GPP_A1	GPP_A1/LAD0/ESPI_IO0	LPC_AD0	Fn 1	+3V3_SS				PU 10K to +3V3_SS (R5675 NS)	
GPP_A2	GPP_A2/LAD1/ESPI_IO1	LPC_AD1	Fn 1	+3V3_SS				PU 10K to +3V3_SS (R5677 NS)	
GPP_A3	GPP_A3/LAD2/ESPI_IO2	LPC_AD2	Fn 1	+3V3_SS				PU 10K to +3V3_SS (R5679 NS)	
GPP_A4	GPP_A4/LAD3/ESPI_IO3	LPC_AD3	Fn 1	+3V3_SS				PU 10K to +3V3_SS (R5681 NS)	
GPP_A5	GPP_A5/FRAME#/SPI_CS0#	LPC_FRAME	Fn 1	+3V3_SS				PU 10K to +3V3_SS (R5675 NS)	
GPP_A6	GPP_A6/SERIRQ/SPI_CLK	LPC_SIRQ	Fn 1	+3V3_SS				PU 10K to +3V3_SS (R5246)	
GPP_A7	GPP_A7/PIRQA#/SPI_ALERT0#	LPC_PIRQA#	Fn 1	+3V3_SS				PU 10K to +3V3_SS (R5248)	
GPP_A8	GPP_A8/CLKRUN#	LPC_CLKRUN_N	Fn 1	+3V3_SS				PU 8.2K to +3V3_SS (R5249)	
GPP_A9	GPP_A9/CLKOUT_LPC0/SPI_CLK	CLK_LPC0_DMI_SS	NC	+3V3_SS					
GPP_A10	GPP_A10/CLKOUT_LPC1		NC	+3V3_SS					
GPP_A11	GPP_A11/PME#/CLKOUT_FME		NC	+3V3_SS					
GPP_A12	GPP_A12/SUS_STAT0#/ESPI_CAT_ERR/DOTF#	SUSWARN#	NC	+3V3_SS					
GPP_A13	GPP_A13/SUSWARN/SUSPWRDNACK	SUSWARN#	Fn 1	+3V3_SS				PU 10K to +3V3_SS (R4698)	
GPP_A14	GPP_A14/SUS_STAT1/ESPI_RESET#	SUS_STAT#	Fn 1	+3V3_SS				PU 10K to +3V3_SS (R5023 NS)	
GPP_A15	GPP_A15/SUSACK#	SUSACK#	Fn 1	+3V3_SS					
GPP_A16	GPP_A16/CLKOUT_48		GPO	+3V3_SS					
GPP_A17	GPP_A17/SD_VISA_CTRL/EMI3/SI_GP7	M.2_WLAN_DISABLE_N	GPO	+3V3_SS				PU +3V3_SS_WLAN (10K R25 M)	HIGH : Disable LOW : Enable
GPP_A18	GPP_A18/I2C_GP0		NC	+3V3_SS					
GPP_A19	GPP_A19/I2C_GP1		NC	+3V3_SS					
GPP_A20	GPP_A20/SI_GP2		NC	+3V3_SS					
GPP_A21	GPP_A21/SI_GP3	M.2_BT_DISABLE_N	GPO	+3V3_SS				PU +3V3_SS_WLAN (10K R24 M)	HIGH : Disable LOW : Enable
GPP_A22	GPP_A22/SI_GP4	TPM_SELECT	GPI	+3V3_SS				100K PD (03002)	HIGH : SW TPM LOW : HW TPM
GPP_A23	GPP_A23/SI_GP5		NC	+3V3_SS					
				Primary Well Group B					
GPP_B0	GPP_B0/GSPI0_CS0#		NC	+3V3_SS					
GPP_B1	GPP_B1/GSPI0_CLK/TIME_SYNC1		NC	+3V3_SS					
GPP_B2	GPP_B2/VRALERT0#_PU	VRALERT0_PU	Fn 1	+3V3_SS				PU 50K to +3V3_SS (R165)	
GPP_B3	GPP_B3/CPU_GP2	BIO_ID5	GPI	+3V3_SS				PU 10K to +3V3_SS (R0726) / PD 10K (R0728)	BORAD ID
GPP_B4	GPP_B4/CPU_GP3		NC	+3V3_SS					
GPP_B5	GPP_B5/SRCCLKREQ5#		NC	+3V3_SS					
GPP_B6	GPP_B6/SRCCLKREQ6#	CLK_REQ7_M.2_WLAN#	Fn 1	+3V3_SS				PU 10K to +3V3_SS (R0727)	
GPP_B7	GPP_B7/SRCCLKREQ7#	CLK_REQ2_LAN#	Fn 1	+3V3_SS				PU 10K to +3V3_SS (R0274)	
GPP_B8	GPP_B8/SRCCLKREQ8#		NC	+3V3_SS					
GPP_B9	GPP_B9/SRCCLKREQ9#		NC	+3V3_SS					
GPP_B10	GPP_B10/I2C1_SCL		NC	+3V3_SS					
GPP_B11	GPP_B11/I2C1_SDA		NC	+3V3_SS					
GPP_B12	GPP_B12/LP_SMI#	PM_ELP_SMI	Fn 1	+3V3_SS					
GPP_B13	GPP_B13/PLTRST_N	PCH_PLTRST_N	Fn 1	+3V3_SS					
GPP_B14	GPP_B14/SPKR	SPKR	Fn 1	+3V3_SS	Top Swap Override	Strap read at rising edge of PCH_PWROK. The internal 20 kohm ± 30% Pull-down is disabled after PCH_PWROK is high.	PD		
GPP_B15	GPP_B15/GSPI0_CS0#		NC	+3V3_SS					
GPP_B16	GPP_B16/GSPI0_CLK		NC	+3V3_SS					
GPP_B17	GPP_B17/GSPI0_MISO		NC	+3V3_SS					
GPP_B18	GPP_B18/GSPI0_MOSI	LPSS_GSPI0_MOSI	Fn 1	+3V3_SS	No Reboot	Strap read at rising edge of PCH_PWROK. The internal 20 kohm ± 30% Pull-down is disabled after PCH_PWROK is high.	PD		
GPP_B19	GPP_B19/GSPI1_CS0#		NC	+3V3_SS					
GPP_B20	GPP_B20/GSPI1_CLK	I2C_SCI#	Fn 1	+3V3_SS				PU 10K to +3V3_SS (R5534)	
GPP_B21	GPP_B21/GSPI1_MISO		NC	+3V3_SS					
GPP_B22	GPP_B22/GSPI1_MOSI	PCH_STRAP_GPP_B22	Fn 1	+3V3_SS	Boot BIOS Strap Bit	Strap read at rising edge of PCH_PWROK. The internal 20 kohm ± 30% Pull-down is disabled after PCH_PWROK is high.	PD		
GPP_B23	GPP_B23/SML1ALERT#/PCHHOT#	SML1ALERT#	Fn 1	+3V3_SS	Intel® DCI OOB Enable	Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% Pull-down is disabled after RSMRST# de-asserts. Note: Do not pull this strap high and strap low, a 1Mk weak board Pull-up is recommended to ensure it does not override the internal Pull-down strap sampling.	PD		
				Primary Well Group C					
GPP_C0	GPP_C0/SMBCLK	SMB_CLK_RESUME	Fn 1	+3V3_SS				PU 2.2K to +3V3_SS (R2025)	
GPP_C1	GPP_C1/SMBDATA	SMB_DATA_RESUME	Fn 1	+3V3_SS				PU 2.2K to +3V3_SS (R2024)	
GPP_C2	GPP_C2/SMBALERT#	SMBALERT#	Fn 1	+3V3_SS	TLS Confidentiality	Native Pf if Intel® SMBus A30 Mode Configuration soft strap = 1, else GP-Out. Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% Pull-down is disabled after RSMRST# de-asserts.	PD		
GPP_C3	GPP_C3/SMLBCLK	SML0_CLK	Fn 1	+3V3_SS				PU 499 ohm to +3V3_S0 (R169)	
GPP_C4	GPP_C4/SMLB0ATA	SML0_DATA	Fn 1	+3V3_SS				PU 499 ohm to +3V3_S0 (R171)	
GPP_C5	GPP_C5/SMLB0ALERT#	SML0ALERT#	Fn 1	+3V3_SS	eSPI or LPC	Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% Pull-down is disabled after RSMRST# de-asserts.	PD		
GPP_C6	GPP_C6/SML1CLK	SML1_CLK	Fn 1	+3V3_SS				PU 2.2K to +3V3_S0 (R173)	
GPP_C7	GPP_C7/SML1DATA	SML1_DATA	Fn 1	+3V3_SS				PU 2.2K to +3V3_S0 (R174)	
GPP_C8	GPP_C8/UART0_RXD		NC	+3V3_SS					
GPP_C9	GPP_C9/UART0_TXD		NC	+3V3_SS					
GPP_C10	GPP_C10/UART0_RTS#		NC	+3V3_SS					
GPP_C11	GPP_C11/UART0_CTS#	CLEAR_CMOS_N	GPI	+3V3_SS					
GPP_C12	GPP_C12/UART1_RXD/SHL0/UART1_RXD		NC	+3V3_SS					
GPP_C13	GPP_C13/UART1_TXD/SHL1/UART1_TXD		NC	+3V3_SS					
GPP_C14	GPP_C14/UART1_RTS#/SHL2/UART1_RTS#	DGPIO_HOLD_RST#	GPO	+3V3_SS				PU 10K to +3V3_S0 (R5412)	
GPP_C15	GPP_C15/UART1_CTS#/SHL3/UART1_CTS#	M.2_SSD_PDET#	GPI	+3V3_SS				PU +3V3_SS_SSD 10K (R1904)	
GPP_C16	GPP_C16/I2C0_SDA	AMP_SDA	Fn 1	+3V3_SS				PU +3V3D_AMP 2.4K (R3720)	
GPP_C17	GPP_C17/I2C0_SCL	AMP_SCL	Fn 1	+3V3_SS				PU +3V3D_AMP 2.4K (R3719)	
GPP_C18	GPP_C18/I2C1_SDA		NC	+3V3_SS					
GPP_C19	GPP_C19/I2C1_SCL		NC	+3V3_SS					
GPP_C20	GPP_C20/UART2_RXD	SSD_PWR_EN	GPO	+3V3_SS					HIGH : POWER on LOW : POWER off S0 states
GPP_C21	GPP_C21/UART2_TXD		NC	+3V3_SS					
GPP_C22	GPP_C22/UART2_RTS#		NC	+3V3_SS					
GPP_C23	GPP_C23/UART2_CTS#		NC	+3V3_SS					
				Primary Well Group D					
GPP_D0	GPP_D0/SPI_CS1/SBK0_BK0		NC	+3V3_SS					
GPP_D1	GPP_D1/SPI_CLK/SBK1_BK1		NC	+3V3_SS					
GPP_D2	GPP_D2/SPI_MISO/SBK2_BK2		NC	+3V3_SS					
GPP_D3	GPP_D3/SPI_MOSI/SBK3_BK3		NC	+3V3_SS					
GPP_D4	GPP_D4/SMB_I2C2_SDA/I2C3_SDA/SBK4_BK4		NC	+3V3_SS					
GPP_D5	GPP_D5/SD3_STRAP/CNV_RF_RESET#	M.2_BT_PCMFRM_CRF_RST_N	Fn 3	+3V3_SS				PD 75 ohm (R22)	
GPP_D6	GPP_D6/SD2_TXD/MODEM_CLKREQ	M.2_BT_PCMOUT_CLKREQ#	Fn 3	+3V3_SS				PD 60.4K (R31)	
GPP_D7	GPP_D7/SD2_RXD		NC	+3V3_SS					
GPP_D8	GPP_D8/SD2_SCLK		NC	+3V3_SS					
GPP_D9	GPP_D9/SPI_SI_CS#/GSPI2_CS0#		NC	+3V3_SS					
GPP_D10	GPP_D10/SPI_SI_CLK/GSPI2_CLK		NC	+3V3_SS					
GPP_D11	GPP_D11/SPI_SI_MISO/GP_BSSB_CLK/GSPI2_MISO		NC	+3V3_SS					
GPP_D12	GPP_D12/SPI_SI_MOSI/GP_BSSB_DI/GSPI2_MOSI		NC	+3V3_SS					
GPP_D13	GPP_D13/SPI_UART0_RXD/I2C2_SDA		NC	+3V3_SS					
GPP_D14	GPP_D14/SPI_UART0_TXD/I2C2_SCL		NC	+3V3_SS					
GPP_D15	GPP_D15/SPI_UART0_RTS#/GSPI2_CS1#/CNV_WFEN		NC	+3V3_SS					
GPP_D16	GPP_D16/SPI_UART0_CTS#/CNV_WCEN		NC	+3V3_SS					
GPP_D17	GPP_D17/DMIC_CLK1/SNDW3_CLK		NC	+3V3_SS					
GPP_D18	GPP_D18/DMIC_DATA1/SNDW3_DATA		NC	+3V3_SS					
GPP_D19	GPP_D19/DMIC_CLK0/SNDW4_CLK		NC	+3V3_SS					
GPP_D20	GPP_D20/DMIC_DATA0/SNDW4_DATA		NC	+3V3_SS					
GPP_D21	GPP_D21/SPI_IO2		NC	+3V3_S0					
GPP_D22	GPP_D22/SPI_IO3		NC	+3V3_SS					
GPP_D23	GPP_D23/SH_I2C2_SCL/I2C3_SCL		NC	+3V3_SS					
				Primary Well Group E					
GPP_E0	GPP_E0/SATAXPCIE0/SATAGP0		NC	+3V3_SS					
GPP_E1	GPP_E1/SATAXPCIE1/SATAGP1		NC	+3V3_SS					
GPP_E2	GPP_E2/SATAXPCIE2/SATAGP2		NC	+3V3_SS					
GPP_E3	GPP_E3/CPU_GP9	GPU_PWR_GOOD	GPI	+3V3_SS				PU 100K +3V3_S0 (R5420)	
GPP_E4	GPP_E4/SATA_DEVSLP0		NC	+3V3_SS					
GPP_E5	GPP_E5/SATA_DEVSLP1		NC	+3V3_SS					
GPP_E6	GPP_E6/SATA_DEVSLP2	WL_CHARGER_DISABLE	GPO	+3V3_SS					HIGH : Disable power LOW : Enable power
GPP_E7	GPP_E7/CPU_GP1	SMBUS_ISP	GPO	+3V3_SS					HIGH : Enable Flash LOW : Disable Flash
GPP_E8	GPP_E8/SATA_LED#_	PCH_SATA_LED_N	Fn 1	+3V3_SS					TEST POINT
GPP_E9	GPP_E9/USB2_OC0#	USB_OC0_N	Fn 1	+3V3_SS				PU 10K +3V3_SS (R91)	
GPP_E10	GPP_E10/USB2_OC1#	USB_OC1_N	Fn 1	+3V3_SS				PU 10K +3V3_SS (R91)	
GPP_E11	GPP_E11/USB2_OC2#	USB_OC2_N	Fn 1	+3V3_SS				PU 10K +3V3_SS (R91)	
GPP_E12	GPP_E12/USB2_OC3#	USB_OC3_N	Fn 1	+3V3_SS				PU 10K +3V3_SS (R111)	
				Primary Well Group F					
GPP_F0	GPP_F0/SATAXPCIE3/SATAGP3		NC						
GPP_F1	GPP_F1/SATAXPCIE4/SATAGP4		NC						
GPP_F2	GPP_F2/SATAXPCIE5/SATAGP5		NC						
GPP_F3	GPP_F3/SATAXPCIE6/SATAGP6		NC						
GPP_F4	GPP_F4/SATAXPCIE7/SATAGP7		NC						
GPP_F5	GPP_F5/SATA_DEVSLP3	FP_RET_N	GPI					PU 10K +3V3_S5 (R5060)	
GPP_F6	GPP_F6/SATA_DEVSLP4	M2_SSD_DEVSLP	Fn 1						
GPP_F7	GPP_F7/SATA_DEVSLP5		NC						
GPP_F8	GPP_F8/SATA_DEVSLP6	GPU_PWR_EN	GPO					PU 100K +3V3_S0 (R5339)	HIGH : Enable power LOW : Disable power
GPP_F9	GPP_F9/SATA_DEVSLP7		NC						
GPP_F10	GPP_F10/SATA_SCLOCK		NC						
GPP_F11	GPP_F11/SATA_SLOAD		NC						
GPP_F12	GPP_F12/SATA_SDATAOUT1		NC						
GPP_F13	GPP_F13/SATA_SDATAOUT0		NC						
GPP_F14	GPP_F14/DDSP_CTRLDATA	PCH_PS_ON	Fn 2						TEST POINT
GPP_F15	GPP_F15/USB2_OC4#	USB_OC4_N	Fn 1					PU 10K +3V3_S5 (0N2) 預留	
GPP_F16	GPP_F16/USB2_OC5#	USB_OC5_N	Fn 1					PU 10K +3V3_S5 (0N2) 預留	
GPP_F17	GPP_F17/USB2_OC6#	USB_OC6_N	Fn 1					PU 10K +3V3_S5 (0N2) 預留	
GPP_F18	GPP_F18/USB2_OC7#	USB_OC7_N	Fn 1					PU 10K +3V3_S5 (0N2) 預留	
GPP_F19	GPP_F19/EXP_VDDEN	UMA_ENVDD	Fn 1						TEST POINT
GPP_F20	GPP_F20/EXP_SMLCTR	SMLEN_PCH	Fn 1						TEST POINT
GPP_F21	GPP_F21/EXP_SMLCTCTL	PCH_ESP_SMLTCTL	Fn 1						
GPP_F22	GPP_F22/DDPF_CTRLCLK		NC						
GPP_F23	GPP_F23/DDPF_CTRLDATA	500K_SI02	GPI	Display Port F Detected	Strap read at rising edge of PCH_PWROK. The internal 20 kohm ± 30% Pull-down is disabled after PCH_PWROK is high.				HIGH : 500K ON LOW : 500K off
				Primary Well Group G					
GPP_G0	GPP_G0/SD_CMD		NC						
GPP_G1	GPP_G1/SD_D0		NC						
GPP_G2	GPP_G2/SD_D1		NC						
GPP_G3	GPP_G3/SD_D2		NC						
GPP_G4	GPP_G4/SD_D3		NC						
GPP_G5	GPP_G5/SD_CLK		NC						
GPP_G6	GPP_G6/SD_WP		NC						
GPP_G7	GPP_G7/SD_RST		NC						
				Primary Well Group H					
GPP_H0	GPP_H0/SRCCLKREQ0#		NC						
GPP_H1	GPP_H1/SRCCLKREQ1#	CLK_REQ7_M.2_SSD#	Fn 1					PU 10K +3V3_SS (R5095)	
GPP_H2	GPP_H2/SRCCLKREQ2#	CLK_REQ8_DGPU#	Fn 1					PU 10K +3V3_SS (R1921)	
GPP_H3	GPP_H3/SRCCLKREQ3#		NC						
GPP_H4	GPP_H4/SRCCLKREQ4#		NC						
GPP_H5	GPP_H5/SRCCLKREQ5#		NC						
GPP_H6	GPP_H6/SRCCLKREQ6#		NC						
GPP_H7	GPP_H7/SRCCLKREQ7#		NC						
GPP_H8	GPP_H8/SRCCLKREQ8#		NC						
GPP_H9	GPP_H9/SRCCLKREQ9#		NC						
GPP_H10	GPP_H10/SML2CLK		NC						
GPP_H11	GPP_H11/SML2DATA		NC						
GPP_H12	GPP_H12/SML2ALERT#	PCH_STRAP_GPP_H12	GP-Out		eSPI Flash Sharing Mode	Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% Pull-down is disabled after RSMRST# de-asserts.	PD		
GPP_H13	GPP_H13/SML3CLK		NC						
GPP_H14	GPP_H14/SML3DATA		NC						
GPP_H15	GPP_H15/SML3ALERT#	GPP_H15	GP-In		Reserved	Strap read at rising edge of RSMRST#. External pull-up is required. Recommend 150 kohm if pulled up to 1.8 V. 1 kohm if pulled up to 1.8 V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.	Z		
GPP_H16	GPP_H16/SML4CLK		NC						
GPP_H17	GPP_H17/SML4DATA		NC						
GPP_H18	GPP_H18/SML4ALERT#		NC						
GPP_H19	GPP_H19/SRCCLKREQ10#		NC						
GPP_H20	GPP_H20/I2C_SCL		NC						
GPP_H21	GPP_H21/I2C_SDA		NC						
GPP_H22	GPP_H22/I2C_SCL		NC						
GPP_H23	GPP_H23/TIME_SYNC0		NC						
				Primary Well Group I					
GPP_I0	GPP_I0/DDPB_HPD0/DISP_MISC0	PCH_HDMIOUT_HPD	Fn 1					PU 1M +3V3_S0 (SR97)	
GPP_I1	GPP_I1/DDPC_HPD1/DISP_MISC1		NC						
GPP_I2	GPP_I2/DDPD_HPD2/DISP_MISC2		NC						
GPP_I3	GPP_I3/DDPE_HPD3/DISP_MISC3		NC						
GPP_I4	GPP_I4/EDP_HPD/DISP_MISC4	EDP_HPD	Fn 1					PD 100K	
GPP_I5	GPP_I5/DDPB_CTRLCLK	PCH_HDMIOUT_CTRLCLK	Fn 1					PU 2.2K +3V3_S0 (R5533)	
GPP_I6	GPP_I6/DDPB_CTRLDATA	PCH_HDMIOUT_CTRLDATA	Fn 1		Display Port B Detected	Strap read at rising edge of PCH_PWROK. The internal 20 kohm ± 30% Pull-down is disabled after PCH_PWROK is high.	PD	PU 2.2K +3V3_S0 (R2031)	
GPP_I7	GPP_I7/DDPC_CTRLCLK		NC						
GPP_I8	GPP_I8/DDPC_CTRLDATA		NC		Display Port C Detected	Strap read at rising edge of PCH_PWROK. The internal 20 kohm ± 30% Pull-down is disabled after PCH_PWROK is high.	PD		
GPP_I9	GPP_I9/DDPD_CTRLCLK		NC						
GPP_I10	GPP_I10/DDPD_CTRLDATA		NC		Display Port D Detected	Strap read at rising edge of PCH_PWROK. The internal 20 kohm ± 30% Pull-down is disabled after PCH_PWROK is high.	PD		
GPP_I11	GPP_I11/M2_SKT2_CFG0	H_SKTOCC_N	GPI					PU 10K +3V3_S5 (R4943)	
GPP_I12	GPP_I12/M2_SKT2_CFG1		NC						
GPP_I13	GPP_I13/M2_SKT2_CFG2		NC						
GPP_I14	GPP_I14/M2_SKT2_CFG3		NC						
				Primary Well Group J					
GPP_J0	GPP_J0/CNV_PA_BLANKING		NC						
GPP_J1	GPP_J1/CPU_VCCIO_PWR_GATE#	CPU_C10_GATE#	Fn 2			The During Reset Pin State of this GPIO is It is a ~ 20 kohm pull-up to 3.3 V independent of soft strap assigned pad voltage. A 1.8 V device connected to this GPIO must be capable of tolerating ~ 20 kohm pull-up to 3.3V.			
GPP_J2	GPP_J_2		NC						
GPP_J3	GPP_J_3		NC						
GPP_J4	GPP_J_4_CNV_BRI_DT_UART0_RTSB	CNV_BRI_DT	Fn 1		XTAL Frequency Select	Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% Pull-down is disabled after RSMRST# de-asserts.	PD		
GPP_J5	GPP_J5/CNV_BRI_RSP/UART0_RXD	CNV_BRI_RSP	Fn 1						
GPP_J6	GPP_J6/CNV_RGI_DT/UART0_TXD	CNV_RGI_DT	Fn 1		M.2 CNV Mode	Strap read at rising edge of RSMRST#. An external pull-up or pull-down resistor is required.	Z		
GPP_J7	GPP_J7/CNV_RGI_RSP/UART0_CTS#	CNV_RGI_RSP	Fn 1						
GPP_J8	GPP_J8/CNV_MFUART2_RXD		NC						
GPP_J9	GPP_J9/CNV_MFUART2_TXD	GPP_J_9_CNV_MFUART2_TXD	GP-Out		1.8 V VCCSPI	Strap read at rising edge of RSMRST#. The internal 20 kohm ± 30% Pull-down is disabled after RSMRST# de-asserts.	PD		
GPP_J10	GPP_J10		NC						
GPP_J11	GPP_J11/AWP_PRESENT		NC						
				Primary Well Group K					
GPP_K0	GPP_K0		NC						
GPP_K1	GPP_K1		NC						
GPP_K2	GPP_K2		NC						
GPP_K3	GPP_K3		NC						
GPP_K4	GPP_K4		NC						
GPP_K5	GPP_K5		NC						
GPP_K6	GPP_K6		NC						
GPP_K7	GPP_K7		NC						
GPP_K8	GPP_K8		NC						
GPP_K9	GPP_K9		NC						
GPP_K10	GPP_K10		NC						
GPP_K11	GPP_K11		NC						
GPP_K12	GPP_K12/GSXDOUT	BIID_ID1	GPI					PU 10K +3V3_SS PD 10K	BORAD ID
GPP_K13	GPP_K13/GSXSLOAD	BIID_ID2	GPI					PU 10K +3V3_SS PD 10K	BORAD ID
GPP_K14	GPP_K14/GSXDIN	BIID_ID3	GPI					PU 10K +3V3_SS PD 10K	BORAD ID
GPP_K15	GPP_K15/GSXSRESET#	BIID_ID4	GPI					PU 10K +3V3_SS PD 10K	BORAD ID
GPP_K16	GPP_K16/GSXCLK	BIID_ID0	GPI					PU 10K +3V3_SS PD 10K	BORAD ID
GPP_K17	GPP_K17/ADR_COMPLETE		NC						
GPP_K18	GPP_K18/NMI#		NC						
GPP_K19	GPP_K19/SMI#	SIO_SCI_N	GPI					PU 10K +3V3_SS (R5305)	
GPP_K20	GPP_K20		NC						
GPP_K21	GPP_K21	SPI_TPM_PIRQ	GPI					PU 10K +3V3_SS (R5505)	CRB Follow
GPP_K22	GPP_K22/MGC1LKOUT0		NC						
GPP_K23	GPP_K23/MGC1LKOUT1		NC						

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Ball Signal	HW Func	Function	HW POWER	External PU / PD	After initial (Default)	S0	S3	S4/S5	
5VSB_CTRL/AGPIRXD/GP16	1st	5VSB_CTRL#	3VSB	10K PU +3V3_DSW_SIO (R8674)		5VSB_CTRL#	5VSB_CTRL#	5VSB_CTRL#	HIGH : 3V/5V_S5 power off LOW : 3V/5V_S5 power on
PCIRSTlink1/CIRTXD/GP15/CPU_PG	3rd	AMP_Mute	???	10K PU +3V3_Scalar (RA27)	GPI	GPI	GPI	GPI	HIGH : AMP Mute on LOW : AMP Mute off
3VSB_3		+3V3_DSW_SIO							
VCORE_EN/PCH_C1/GP14	3rd	SIO_SMBLINK1_CLK	VCC3	10K PU +3V3_S5 (R173)		PCH_C1	PCH_C1	PCH_C1	
SLP_SUS#/VOLT_EN/GP63		SLP_SUS#	3VSB	PD 100K (R8710)		SLP_SUS#	SLP_SUS#	SLP_SUS#	給收 PCH 當成到 SLP_SUS#
GNDD_6		GND							
FAN_TAC1		SYS_FAN_TACH							
FAN_CTL1		SYS_FAN_PWM							
FAN_TAC2/GP62	2nd	EC_1.05V_EN	3VSB	10K PU +3V3_DSW_SIO (R8682)	GPO	GPO/HIGH	GPO/HIGH	GPO/HIGH Deep sleep S5 : LOW	給收到 3V5V_PG 後 HIGH : Power on (+1V05_S5) LOW : Power off (+1V05_S5)
FAN_CTL2/GP51	2nd	VR_PWRGD	3VSB	1K PU +3V3_S0 (R8391)	GPI	GPI	GPI	GPI	給收 VR_POWER GOOD 訊號 HIGH : Power on LOW : Power off
FAN_TAC3/GP57	2nd	SIO_SCI_N	3VSB	10K PU +3V3_S0 (R8335)	GPO				
FAN_CTL3/GP36	2nd	USB_SIDE_EN	3VSB	10K PU +3V3_DSW_SIO (R8729)	GPO	GPO/HIGH	GPO/LOW	GPO/LOW	跟隨 PM_SLP_S4# 做(依管理韌韌行調整) HIGH : Power on LOW : Power off
F_DIO3/GP35		NC							
DPWROK/GP32	1st	DSW_PWRGD_EC	3VSB	1K PU +3V3_DSW_SIO (R8644)		DPWROK	DPWROK	DPWROK	發送 DSW_PWRGD_EC 訊號 給 PCH HIGH : power on LOW : power off
VFSPI		+3V3_DSW_SIO							
F_DIO3/GP30	2nd	HDMI_IN_DET	???	10K PU +3V3_DSW (R8644)	GPI	GPI	GPI	GPI	給收 HDMI_IN_DET 訊號 HIGH : no cable det LOW : cable det
SIN3/GP27	1st	3VSV_PG	3VSB	10K PU +3V3_DSW_SIO (PR225)	GPI	GPI	GPI	GPI	給收 3V5V_PG 訊號 HIGH : Power on LOW : Power off
SOUT3/GP26	1st	HW_12V_S0_EN	3VSB	10K PU +3V3_S0 (R8689)	GPO	GPO/HIGH	GPO/LOW	GPO/LOW	跟隨 PM_SLP_S3# 做(依管理韌韌行調整) HIGH : Power on LOW : Power off
DSR3/GP25	1st	MB_DIS_SIO	3VSB	10K PU +3V3_S5 (R819)	GPO				LOW : Active
RTS3#/GP24	1st	+3V3_DSW_SCR_EN	3VSB	10K PU +3V3_DSW_SIO (R8730)	GPO	GPO/HIGH	HIGH : Cable Det	HIGH : Cable Det	S5-S0狀態下，跟隨 PM_SLP_S3# 做給 HIGH 狀 況出現HIGH 時 表 示 偵測 HDMI_IN_DET 訊號
SI/GP23	1st	SIO_SI	3VSB			SI	SI	SI	
SCK/GP22	1st	SIO_SCK	3VSB			SCK	SCK	SCK	
DCD2#/GP21	1st	SIO_GPIO_21	3VSB		???	SIO_GPIO_21	SIO_GPIO_21	SIO_GPIO_21	
CTS2#/GP20	1st	Type-C_ID	3VSB	200K PU +5V_CC (R8624)	GPI	GPI	GPI	GPI	偵測 Type-C CONN 連接 HIGH : NO CONN LOW : CONN
RI2#/GP17	2nd	Type-C_EN	3VSB	10K PU +3V3_S5 (R8774)	GPO	GPO	GPO	GPO	AND 閘 PM_SLP_S4# / Type-C_ID 1 : 0 LOW 動作 正值 HIGH 動作
DTR2/GPA7	2nd	USB_REAR_EN	3VSB	10K PU +3V2_DSW_SIO (R8672)	GPO	GPO/HIGH	GPO/LOW	GPO/LOW	跟隨 PM_SLP_S4# 做(依管理韌韌行調整) HIGH : Power on LOW : Power off
CE_N/CRTX1		SIO_CS_N	3VSB			CE_N	CE_N	CE_N	
SO/GP50	1st	SIO_SO	3VSB			SO	SO	SO	
PWRGD1/GP13	2nd	PCH_PWROK	VCC3	10K PU +3V3_S0 (R8731)	GPO	GPO/HIGH	GPO/LOW	GPO/LOW	給收 VR_PWRGD 後 (依管理韌韌行調整) HIGH : PWROK on LOW : PWROK off
PCIRST1#/POH_D1/GP12	2nd	SIO_SMLINK1_DATA	VCC3	10K PU +3V3_S0 (R174)		PCH_D1	PCH_D1	PCH_D1	
PCIRST2#/GP11	2nd	PANEL_ID2	3VSB	10K PU +3V2_DSW_SIO (R8162)	GPI	GPI	GPI	GPI	偵測 Panel ID2
3VSB_32		+3V3_DSW_SIO							
VCORE		VCORE							
VCCBT		+3V3_DSW_SIO							
GNDD_35		GND							
ESPI_ALERT1/SERIRQ		SERIRQ	VCC3						
ESPI_CS#/LFRAME#		LPC_FRAME#	VCC3						
ESPI[0]/LAD0		LPC_AD0	VCC3						
ESPI[1]/LAD1		LPC_AD1	VCC3						
ESPI[2]/LAD2		LPC_AD2	VCC3						
ESPI[3]/LAD3		LPC_AD3	VCC3						
CLKIN_ENRST#		KBRST_N	VCC3						
ESPI_RESET#/GA20/GPB2		NC							
ESPICLK/PCICLK		CLK_LPC0_24M_SIO	VCC3						
LDRQ/GPB2	1st	LPC_DRQ0#	VCC3			LDRQ	LDRQ	LDRQ	
PLTRST#/LRESET#		PCH_PLTRST_N	VCC3						
WRST#		WRST#	3VSB	100K PU +3V3_DSW_SIO (R8734) 1uF PD (C8539)					
SMBCLK1/GP68		SMBCLK1/GPB8	3VSB						FOR DEBUG
SMBDAT1/GP66		SMBDAT1/GPB6	3VSB						Pull up to 3V3_DSW
SST/AMDTSI_O/GP62	2nd	SYS_PWROK	???	10K PU +3V3_DSW_SIO (R8673)	GPO	GPO/HIGH	GPO/LOW	GPO/LOW	給收 PWRGD_PSU_SIO (以提供+3V3_S0) 後 發出HIGH 訊號 (依管理韌韌行調整) HIGH : POWER ON LOW : POWER OFF
PECI/AMDTSI_O/GP64	1st	H_PECI	VCC3						
PWM0/UT0/GP31	2nd	PWRBTN_LED	3VSB	10K PU +3V3_S5	GPO	GPO/HIGH	GPO/Flash	GPO/LOW	Power LED S0 : S0 or co already ME S1 / S3 : S0 Blinke 1Sec/st S4 / S5 : S0 Off
PWM1/UT1/GP40	2nd	PCIE_WAKE#	3VSB	10K PU +3V3_S5_LAN (R8537)	GPI	GPI	GPI	GPI	給收 PCIE_WAKE# LOW : Reset on HIGH : Reset off
USB1W1_DM		USB2_P1_SIO_DP	3VSB						From PCH
USB1W1_DP		USB2_P1_SIO_DN	3VSB						
USB1W1_YM		USB2_P1_SIO_CON_DP	3VSB						TO USB Type-A CONN
USB1W1_YP		USB2_P1_SIO_CON_DN	3VSB						
GP66/SMBCLK0	2nd	SMB_CLK_SUS	3VSB			SMBCLK0	SMBCLK0	SMBCLK0	TO GPU SMB
IO_SCI#/GP65/SMBDAT0	3rd	SMB_DATA_SUS	3VSB			SMBDAT0	SMBDAT0	SMBDAT0	
SMBDAT2/GP47		VCCIO_PGD	???		GPI	GPI	GPI	GPI	給收 VCCIO_PGD 訊號 HIGH : POWER ON LOW : POWER OFF
SMBCLK2/GP46		NC	???						
CLK125M		SIO_CLK125K	3VSB						
CLK32KHZ		SIO_CLK32K	3VSB						
3VSB_R4		+3V3_DSW_SIO							
COPEN#		COPEN#							
VBAT		+3V3_VBAT							
SYS_3V5B		EC_PCHV5B							
SUSB#/GP48		PM_SLP_S3#	3VSB			PM_SLP_S3#	PM_SLP_S3#	PM_SLP_S3#	給收 PCH 端的 SLP_S3# 訊號
PWROK#/GP44		PBTN_OUT#	3VSB	10K PU +3V3_DSW_SIO (R8735)		PBTN_OUT#	PBTN_OUT#	PBTN_OUT#	給收到開機訊號 ON/OFF# 後 發送 PBTN_OUT# 給 PCH
PME#/GP54/USPWREN1#		EC_SCI#	3VSB			EC_SCI#	EC_SCI#	EC_SCI#	
GNDD_71		GND							

FANSWH#/GP43		ON/OFF#	3VSB	10K PU +3V3_DSW (R2656)		ON/OFF#	ON/OFF#	ON/OFF#	給收 風扇開消訊號
PSON#/GP42		EC_GP42	3VSB	4.7K PU +3V3_DSW_SIO (R5894)		EC_GP42	EC_GP42	EC_GP42	
SUSC#/GP52		PM_SLP_S4#	3VSB			PM_SLP_S4#	PM_SLP_S4#	PM_SLP_S4#	給收 PCH 端的 SLP_S4# 訊號
PWROK2/GP41/SDA	1st	PWROK2 / EC_RSMRST#	VCC3						做Mirror share ROM 時控制 EC_RSMRST# 訊號
3VSB3/WUI2/GP53/SCL		EC_CRX0/1	3VSB	4.7K PU +3V3_DSW_SIO (R5409)					
KDA1/GPA1		EC_CRX0/1_KSO0	3VSB	10K PU +3V2_DSW_SIO (R5668)					
KCL4/GP60		KCL4/GP60	3VSB	10K PU +3V2_DSW_SIO (R5694)					
MDA1/GP67	2nd	H_PROCHOT_SIO#	3VSB	10K PU +3V2_DSW_SIO (R5158)	GPO	H_PROCHOT_SIO#	H_PROCHOT_SIO#	H_PROCHOT_SIO#	發送 H_PROCHOT_SIO# 給 PCH端
MCLK/GP56		MCLK/GP56	3VSB	10K PU +3V3_DSW_SIO (R5693)					
PCIRST3#/GP10	1st	SIO_PCIRST3#	VCC3	10K PU +3V3_S0 (R493)		SIO_PCIRST3#	SIO_PCIRST3#	SIO_PCIRST3#	發送 SIO_PCIRST3# 到 TPM 的RST 動作 LOW : Reset on HIGH : Reset off
RSMRST#/CIRRX1/GP55	1st	EC_RSMRST#	3VSB	1K PU +3V3_S5 (R812)		EC_RSMRST#	EC_RSMRST#	EC_RSMRST#	給收 +1V05_S5_PGOOD_R 後 發送 HIGH 訊號 到延 PD 10K (R8734)
GNDA		GND							
TSD-		SIO_TSD-							
TMPIN3		VRM_THERMDA							
TMPIN2		GPU_VR_SSD_THERMDA							
TMPIN1		SYS_THERMDA							
VREF		SIO_VREF							
VCC3DET		SIO_VCC3DET		1K PU +3V3_S0 (R496)	PWR IN				判斷 +3V3_S0 存/電訊來方
VIN5/5VSB_SEN		NC							
VIN4/VLDT_12		NC							
VIN3		NC							
VIN2		NC							
VIN1/VDIMM_STR(1.2V)		NC							
VIN0/VCORE(0.8V)		+VCCST_VCCPLL_S3_EC			PWR IN				判斷 +VCCST_VCCPLL_S3 是/不存/電 訊號 : 1.05V
A3VSB		+3V3_A3VSB_SIO							
GPI0		BRD_ID1	???	10K PU +3V3_S0 (R131)	GPI	GPI	GPI	GPI	給收PCH端 BRD_ID1 訊號 HIGH : 7/GPU LOW : 10/GPU
GPI4/ATXPG		PWRGD_PSU	3VSB	10K PU +3V3_S0 (R8166)	GPI	GPI	GPI	GPI	判斷 +3V3_S0 存/電訊來方
GPI5/FAN_TAC4		VCCSA_EN#	3VSB	10K PU +3V3_DSW_SIO (R8341)	GPO	GPO/HIGH	GPO/LOW	GPO/LOW	跟隨 VR_ON 後發送訊號 LOW : POWER ON HIGH : POWER OFF
GPI6		LPC_CLKRUN_N		8.2K PU +3V3_S0 (R149)		LPC_CLKRUN_N	LPC_CLKRUN_N	LPC_CLKRUN_N	LPC_CLKRUN_N
SLCT/GPI57	2nd	PANEL_ID0	3VSB	10K PU +3V3_DSW_SIO (R8160)	GPI	GPI	GPI	GPI	偵測 PANEL_ID0
PE/GPI56	2nd	PANEL_ID1	3VSB	10K PU +3V3_DSW_SIO (R8161)	GPI	GPI	GPI	GPI	偵測 PANEL_ID1
BUSY/GPI61		+1V05_S5_PGOOD_R	3VSB	10K PU +3V3_S5 (PR1376)	GPI	GPI	GPI	GPI	給收 +1V05_S5_PGOOD_R 電壓 : 3V3 HIGH : POWER ON LOW : POWER OFF
ACK#/GPI62		PM_SLP_S0#	3VSB		GPI	PM_SLP_S0#	PM_SLP_S0#	PM_SLP_S0#	給收 PCH 端的 SLP_S0# 訊號
SLIN#/GPI60		UART4_P80_EN	VCC3	100K PD (R8760)	GPI	GPI	GPI	GPI	給收 UART4_P80_EN 訊號 HIGH : Debug mode LOW : USB mode
INIT#/GPI64		NC	VCC3						
ERR#/GPI97		NC	VCC3						
AFD#/GPI90		EC_INT_BL	???	4.7K PU +3V3_Scalar_S5 (R8762)	GPI	GPI	GPI	GPI	給收 EC_INT_BL 訊號 (前期) HIGH : no active LOW : INT
STB#/GPI91		NC	???						
KSI0/GPI70/PD0	2nd	Detect gpu	3VSB	10K PU +3V3_S0 (R8780)	GPO	GPO	GPO	GPO	給收到 BRD_ID1 後 發送 訊號 HIGH : 7/GPU LOW : 10/GPU
KSI1/GPI71/PD1	2nd	EC_RTCRST	3VSB	10K PU +3V3_DSW_SIO (R8781)	GPO	GPO	GPO	GPO	從 ON/OFF 信號 (LOW 8~10秒) 後 發出HIGH 訊號
KSO0/GPI72/PD2	2nd	WLAN_PWR_EN	3VSB	10K PU +3V3_DSW_SIO (R8671)	GPO	GPO/HIGH	GPO/LOW	GPO/LOW	跟隨 PM_SLP_S4# 做(依管理韌韌行調整) HIGH : Power on LOW : Power off
KSO1/GPI73/PD3	2nd	SUSPF	3VSB	10K PU +3V3_DSW_SIO (R8346)	GPO	GPO/HIGH	GPO/LOW	GPO/LOW	跟隨 PM_SLP_S3# 做(依管理韌韌行調整) HIGH : Power on LOW : Power off
KSO2/GPI74/PD4	2nd	ADP_PROTECT	3VSB	10K PU +3V3_S0	GPI	GPI	GPI	GPI	由 POWER Page 給收SPEC檢驗者
KSO3/GPI75/PD5	2nd	RMT_FAN_DISABLE#	3VSB		GPO				進入 S0X0 時於 LOW HIGH : Active LOW : Power off
KSO4/GPI76/PD6	2nd	ADP_OCP_EN	3VSB	4.7K PU +3V3_DSW_SIO	GPO	GPO/HIGH	GPO/HIGH Deep sleep S5 : LOW	GPO/HIGH Deep sleep S5 : LOW	給收到 3V5V_PG 後 發出HIGH EN 訊號
KSO5/GPI77/PD7	2nd	VR_ON	3VSB	4.7K PD	GPO	GPO/HIGH Entry S0IX LOW	GPO/LOW	GPO/LOW	給跟隨(S3) PM_SLP_S3# VCCIO_PGD 1 1 : HIGH 10/01/00 : LOW
SMBCLK4		EC_SMLCLK_BL	3VSB			SMBCLK4	SMBCLK4	SMBCLK4	跟隨線路
SMBDAT4		EC_SMLDAT_BL	3VSB			SMBDAT4	SMBDAT4	SMBDAT4	跟隨線路
FAN_CTL4/GP67		NC	3VSB						
RTS1#/GPB0	2nd	S0IX_POWER_EN	3VSB	10K PU +3V3_S5 (R8690)	GPO				S0IX 動作 (跟隨) HIGH : Active LOW : POWER Saving
DSR1#/GPB1	2nd	SYSON	3VSB	4.7K PU +3V3_DSW_SIO (R5382)	GPO	GPO/HIGH	GPO/HIGH	GPO/LOW	跟隨 PM_SLP_S4# 做(依管理韌韌行調整) HIGH : Power on LOW : Power off
SOUT1/D_TX1/JP3		JP3_EC	VCC3						Straping
SIN1/D_RX1/GPB3	3rd	SUSWARN#	3VSB	1K PD	GPI	GPI	GPI	GPI	給收 SUSWARN# 訊號
DTR1#/GPB4/JP2		JP2_EC	3VSB	PU 1K +3V2_DSW_SIO (R8768) PD 680 ohm (第一張原理表上件)	GPO				Straping
DCD1#/GPB6	2nd	VCCST_PWRGD_EC	3VSB	1K PU +VCCST_VCCPLL_S3 (R9681)	GPO	GPO/HIGH	GPO/LOW	GPO/LOW	給收 VR_PWRGD 後 發送(依管理韌韌行調整) HIGH : POWER ON LOW : POWER OFF
RI1#/GPB6		NC	3VSB						
CTS1#/GPB7	2nd	SUSACK#	3VSB		GPO	GPO	GPO	GPO	給收 SUSWARN# 後 發送

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Title: P78 ESIO GPIO Table

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ET to SDV

Page 62 1V8_S5
PR7145 change to 433-010884-01A 102K 0402 1%
PC6917&PC6918 change to 432-010193-01A MLCC 22uF 6.3V +/-10% X5R 0805

Page 69 VCCIA
PL67 Change to 437-020005-01A BEAD 80ohm +/-25% 6A 0.01ohm 0805 100MHz SMT*3 pcs

Page 73 VCCSA
PR305 Change to 433-013803-01A R-CHIP 7.5Kohm 1% 1/10W 0603
PL1110 change to 1UH

Page 62 1V8_S5
PC7089 change to I

Page 66 1V05_S3
PC7083 change to I

Page C67 12V_S0
PC340 change to I

Page 74 10V_LVDS
PC1177 change to I

Page 28 M.2 Wifi
R1319 R1317 change 49.9ohm

Page 73 VCCSA
PL2 Change to 437-010350-01A INDUCTOR 0.36uH +/-15% 100KHZ 50A 1.05mohm SMT SRPN1004-R36L-D-1D05E
PEC67 Change NI
PR329 Change to 433-010057-01A R-CHIP 4.02Kohm 1% 1/16W 0402
PC7105 Change to 432-010170-01A MLCC 2200pF 50V +/-10% X7R 0402
PR300 Change to 433-010330-01A R-CHIP 88.7Kohm 1% 1/16W 0402
PC7202 Change to 432-011973-01A MLCC 3900pF 50V +/-10% X7R 0402
PC7203 Change to 432-011846-01A MLCC 0.039uF 25V +/-10% X7R 0402

Page 68
PR359 Change to 433-010411-01A R-CHIP 127Kohm 1% 1/16W 0402
PC7217 Change to 432-010024-01A MLCC 1500pF 50V +/-10% X7R 0402
PR7195 Change to 433-011162-01A R-CHIP 133Kohm 1% 1/16W 0402
PR353 Change to 433-012628-01A R-CHIP 35.7Kohm 1% 1/16W 0402
PC7147 Change to 432-010024-01A MLCC 1500pF 50V +/-10% X7R 0402
Page 18
R165 change to NI (IPT MODE)
Page 72
PR7135 change to I(+VCCIO_LPM# pull high)
Page 68
PR2383 change to NI(+VCCIO_0_PG_R)
Page 20
Change BT_P/N singal
Page 48
EC_GP20 pull high 3v3_S5
Page 75
PEC3 colay PEC86
Page 76
Change the enable source for AMP power

Page 76
PC1694 Change to 432-010339-01A MLCC 0.047uF 25V +/-10% X7R 0402

Page 09
 BCLK PCI_BCLK CLK24 M2_WIFI_100M_CLK add the damping for SI test

Page 57
ADD Bleed off for VR_ON , VCCIO_EN (Sequence)

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RESERVED

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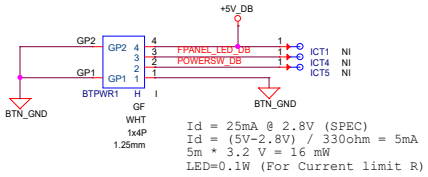
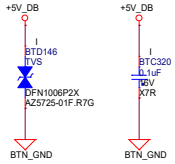
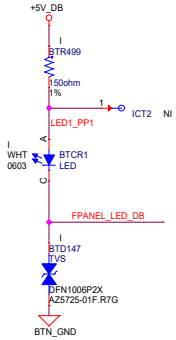
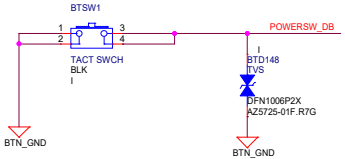
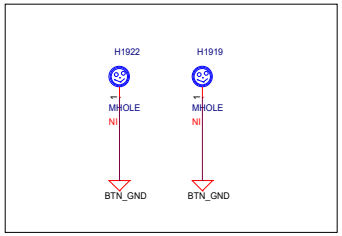








	S0/S1	S3	S4/S5
LED STATE	ON	BLINKING	OFF



AVC	Asia Vital Components Co., Ltd.	
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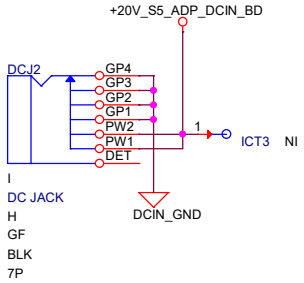
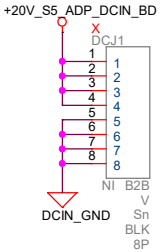
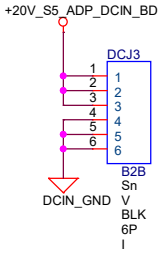
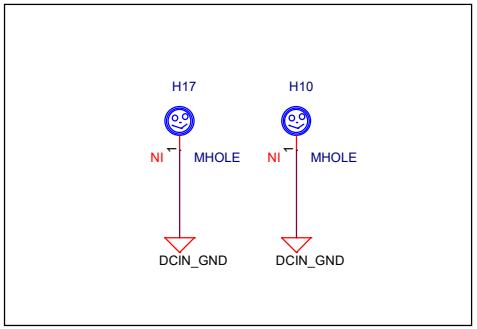
DC Board









Asia Vital Components Co., Ltd.		
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